A Hybrid Seven Level Inverter Topology with a Single DC Supply and Reduced Switch Count

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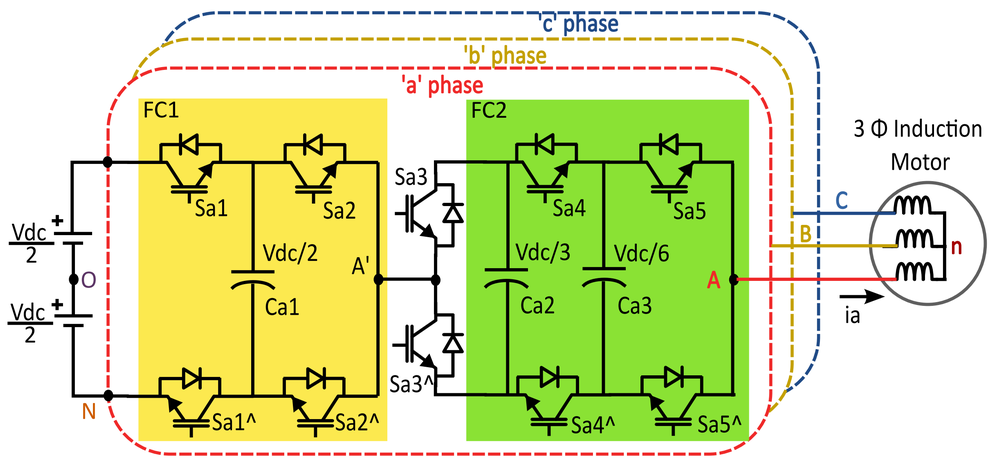
Abstract

A new **three-phase hybrid seven level inverter** topology with a **single DC supply** is proposed for the first time. The proposed inverter is realised by cascading two three-level flying capacitor inverters with a half bridge module. The inverter topology has switching state redundancies for each of the pole voltage level. By using these switching state redundancies, **capacitor charge can be controlled in every PWM switching cycle**. This feature is advantageous for reducing the capacitor size. Another advantage of the proposed inverter is that the charge balancing of each **capacitor can be controlled irrespective of the modulation index and the load power factor**. A hysteresis based capacitor charge control algorithm is implemented for the proposed inverter. Furthermore, the proposed topology uses **lesser number of semiconductor devices, capacitors and DC power supplies** compared to conventional seven level inverter topologies.

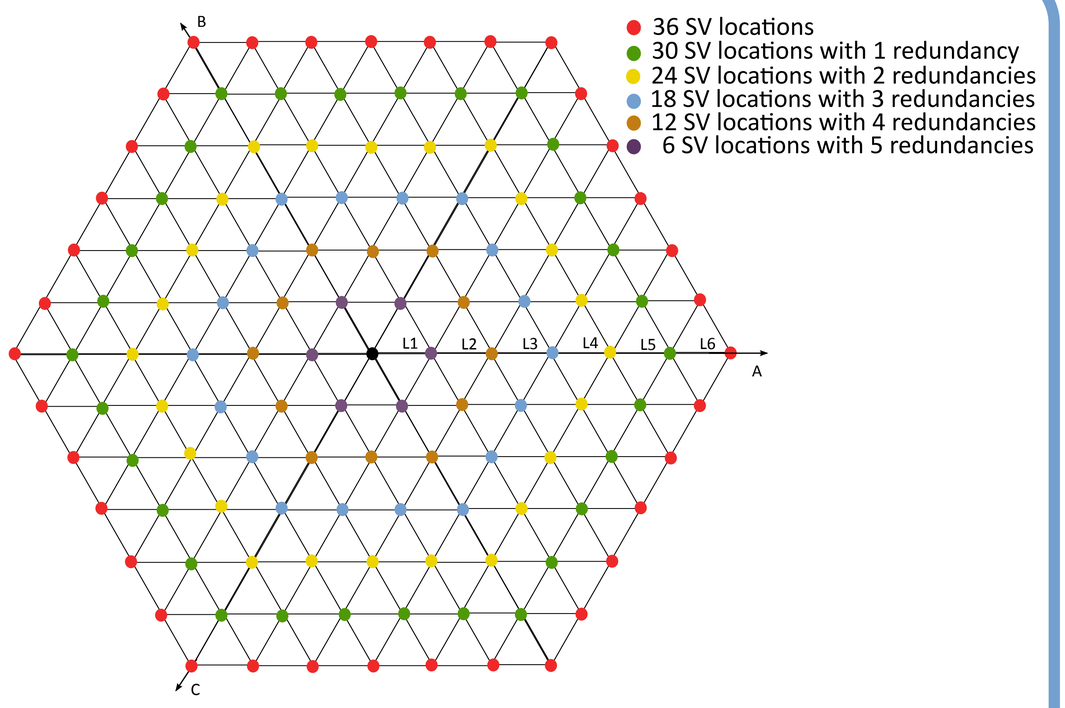
Inverter Topology

Seven level inverter power circuit



- A seven level inverter is realised by cascading two three level flying capacitor inverters
- Reduced switch count and single DC supply requirement
- Capacitor balancing over a switching cycle irrespective of load power factor
- Reduced capacitor sizing for a given power level
- Tight control of capacitor voltage for over modulation operation

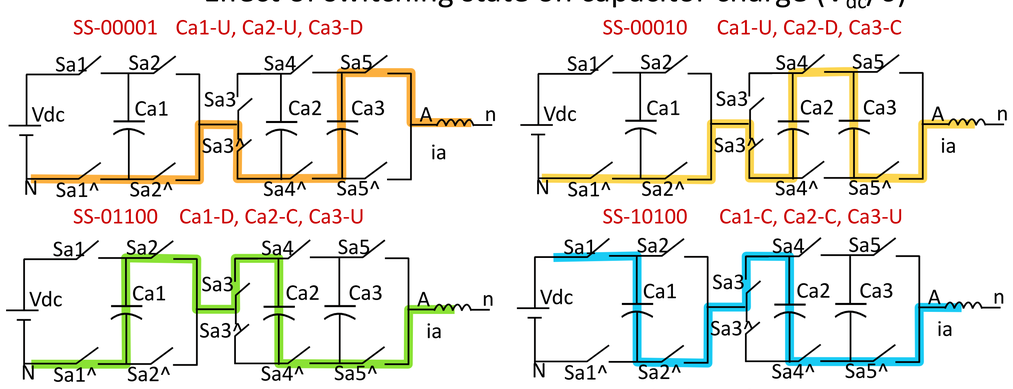
Space Vector Diagram



- 343 pole voltage combinations
- 127 space vector locations with six hexagonal layers

Capacitor Voltage Balancing

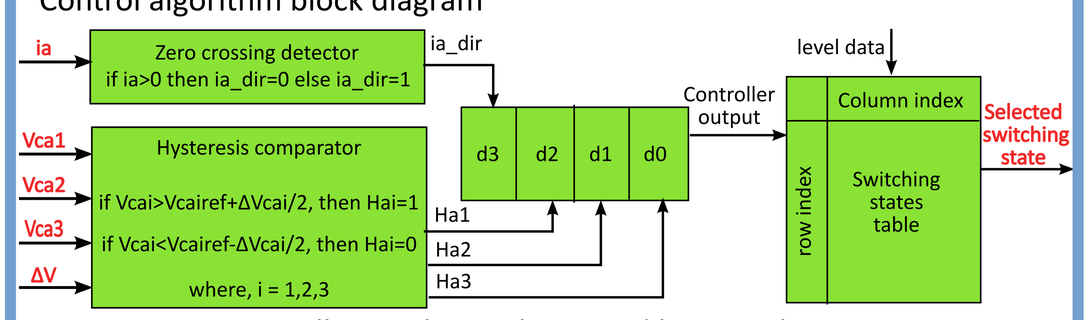
Effect of switching state on capacitor charge ($V_{dc}/6$)



Pole voltage (V_{AN}) = $V_{dc}/6$

U - Unaffected, D - Discharging, C - Charging

Control algorithm block diagram



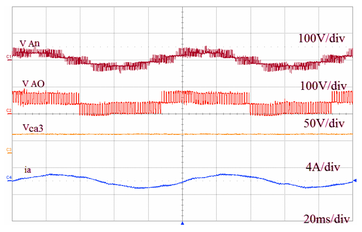
- Hysteresis controller can be implemented by using low cost opamp comparators
- Capacitor charge balance irrespective of load current power factor and modulation index

Experimental Results

Steady state results

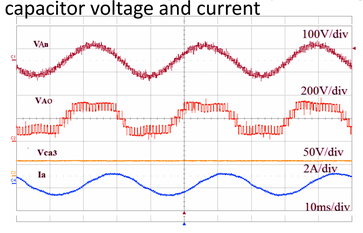
10 Hz operation

Motor phase voltage, inverter pole voltage capacitor voltage and current



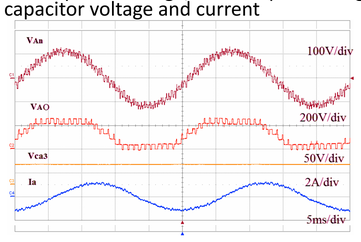
30 Hz operation

Motor phase voltage, inverter pole voltage capacitor voltage and current



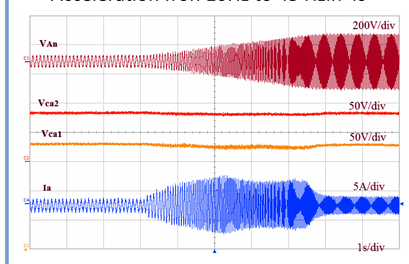
40 Hz operation

Motor phase voltage, inverter pole voltage capacitor voltage and current

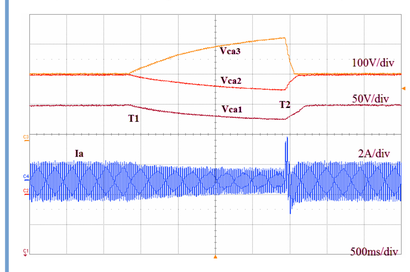


Transient operation

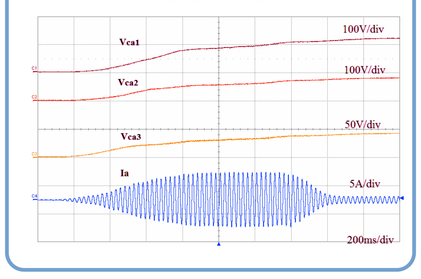
Acceleration fron 10Hz to 45 Hzin 4s



Capacitor voltage controller stability test



Capacitor charging during inverter turn on



Conclusion

- The key advantages of proposed topology are- Reduced number of switches, **Reduced capacitor sizing, Single DC supply** requirement and Less switching for higher voltage devices
- A hysteresis controller based capacitor voltage balancing scheme which **does not require any pre-charging circuitry for startup**
- **Capacitor voltage balancing irrespective of the load current power factor** and direction for all modulation indices including over-modulation, 36- step operation and transient operations

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