A Hybrid Seven Level Inverter Topology with a Single DC Supply and Reduced Switch Count

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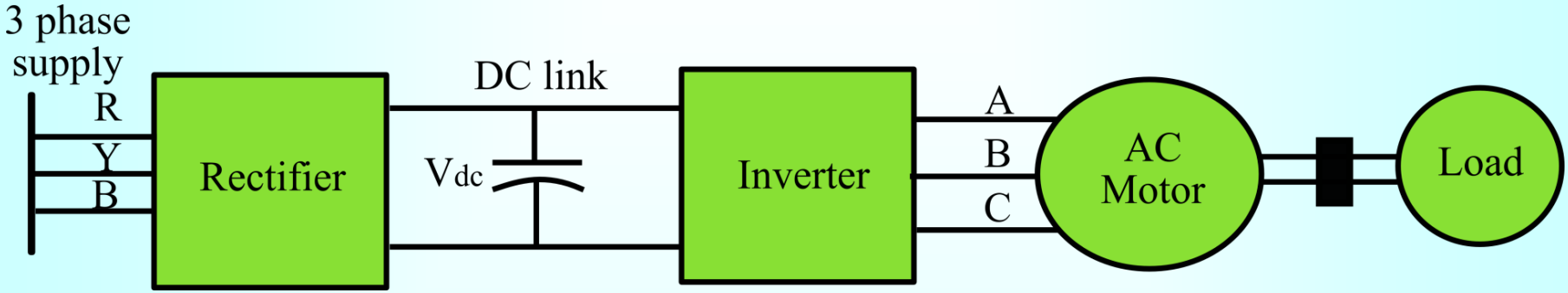
Overview of presentation

- Adjustable speed AC drive systems
- Inverter topologies
- New seven level inverter topology
- Experimental results

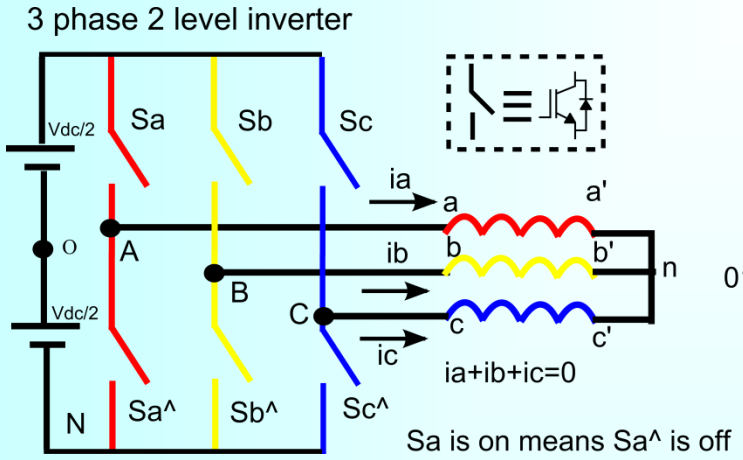
Adjustable speed AC drive system

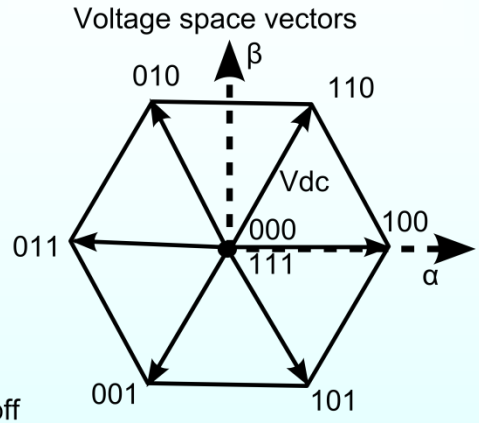


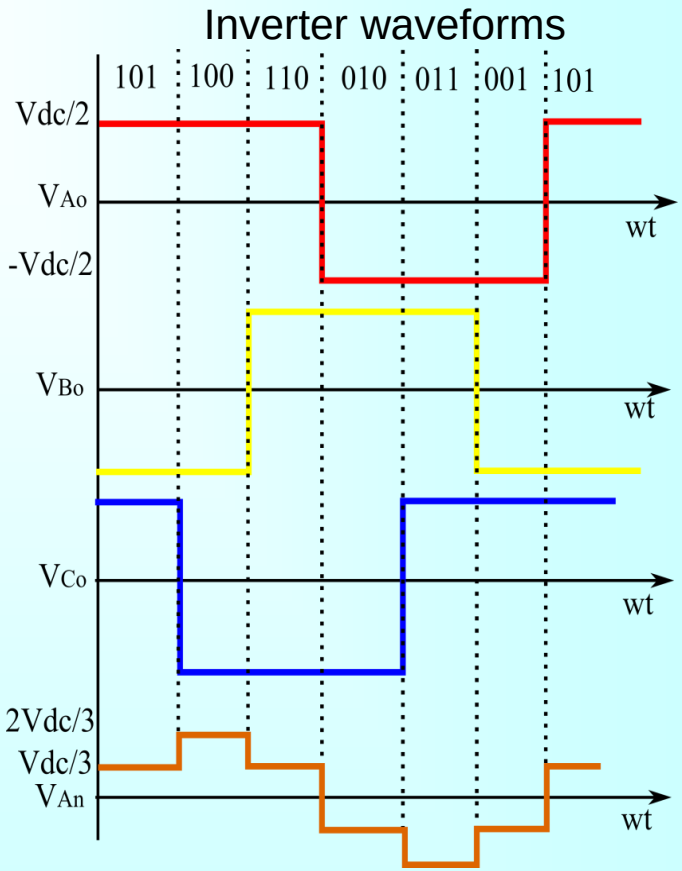
Important modules of an adjustable speed AC drive system are,

- Rectifier
- Three phase Inverter
- AC motor

3 phase two level Inverter







- There are 8 (2^3) valid switching states are possible
- Less number of devices

- V_{Ao} is defined as inverter pole voltage.
- V_{An} is defined as motor phase voltage.

Multilevel inverter topologies

Important advantages of multilevel inverters are,

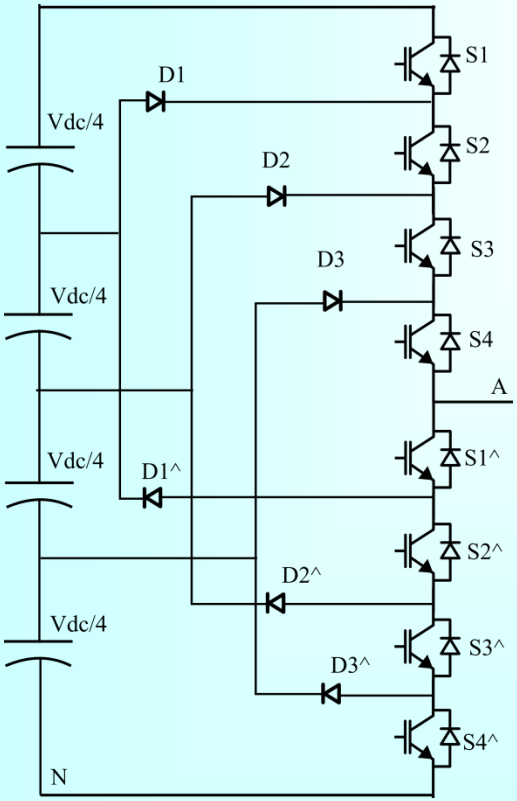
- Reduced switching frequency
- Reduced EMI
- Improved voltage and current THD
- Reduced filtering requirements

Commonly used multilevel inverter topologies are,

- Diode clamped inverter
- Flying capacitor inverter
- Cascaded H-bridge inverter
- Hybrid multilevel inverter

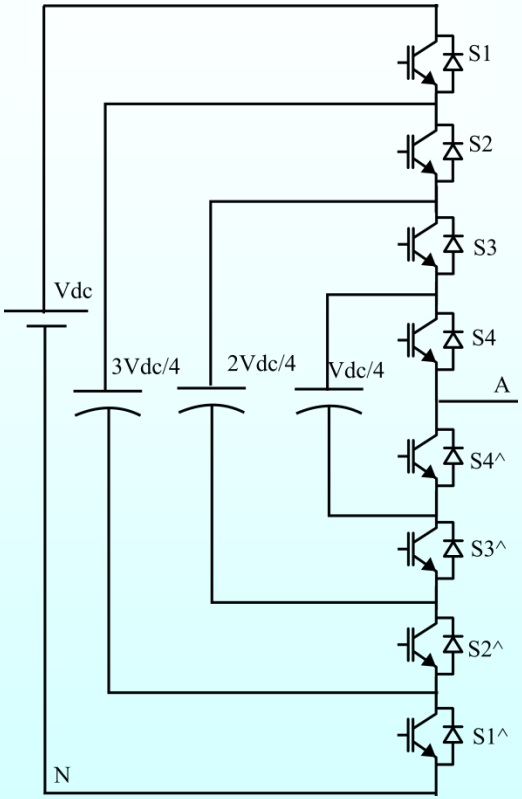
Multilevel inverter topologies

5 level diode clamped inverter



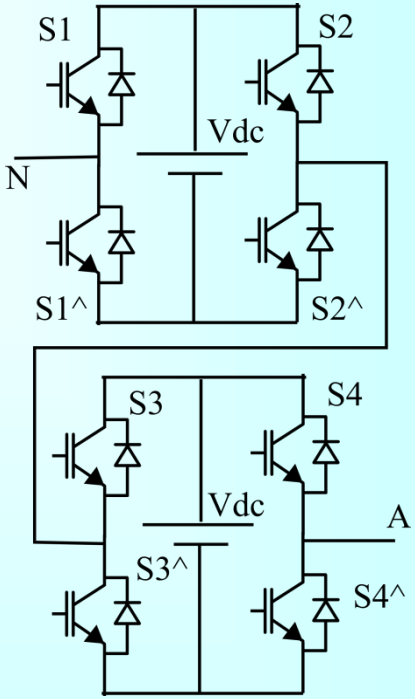
- Requires clamping diodes
- DC link capacitor voltage balancing is difficult

5 level flying capacitor inverter



- As the number of voltage levels increases capacitor voltage balancing is difficult

5 level cascaded H-bridge inverter



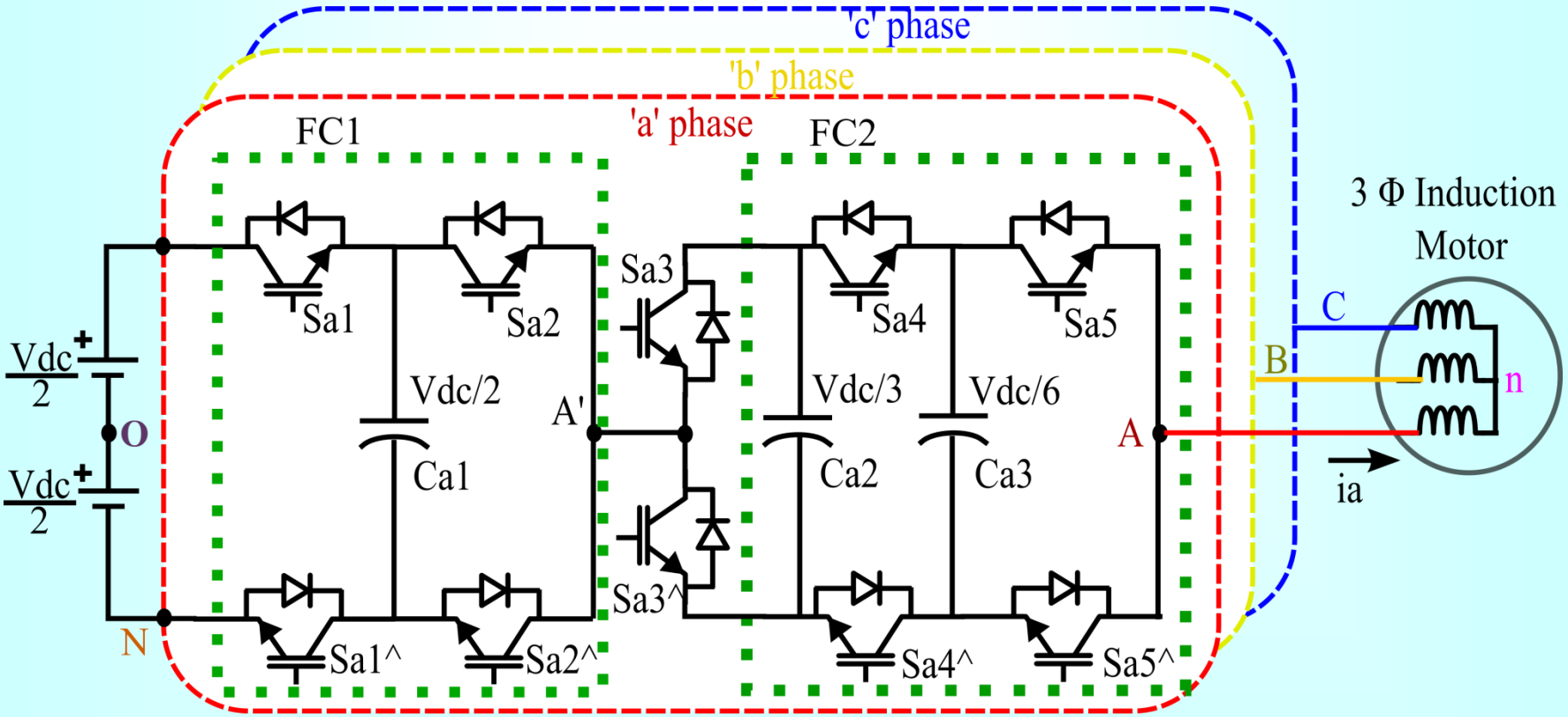
- Modular structure
- Requires multiple DC supply for operation

Motivation for research

To develop a new multilevel inverter topology :

- With single DC supply
- Satisfactory over modulation operation
- Minimum number of switching devices
- Reduction in capacitance values

Proposed seven level inverter topology

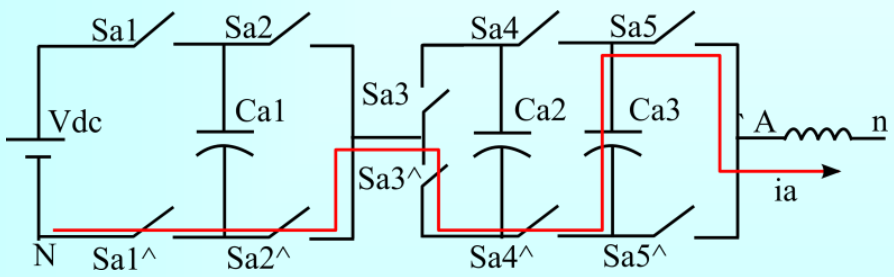


- The proposed topology is realized by cascading two three level flying capacitor inverter using a half bridge module.

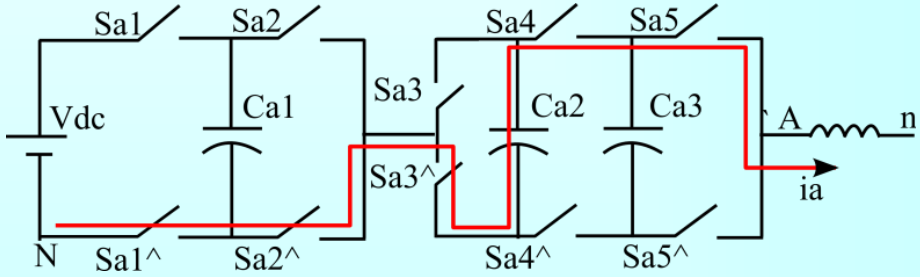
Analysis of inverter topology

- Five pair of complementary switches with 32 switching state for each phase.

- The inverter can generate 11 pole voltage levels:
  $-5V_{dc}/6$, $-4V_{dc}/6$, $-3V_{dc}/6$, $-2V_{dc}/6$, $-V_{dc}/6$, 0, $V_{dc}/6$, $2V_{dc}/6$, $3V_{dc}/6$, $4V_{dc}/6$ and **$5V_{dc}/6$** with respect to DC bus mid point ‘O’.

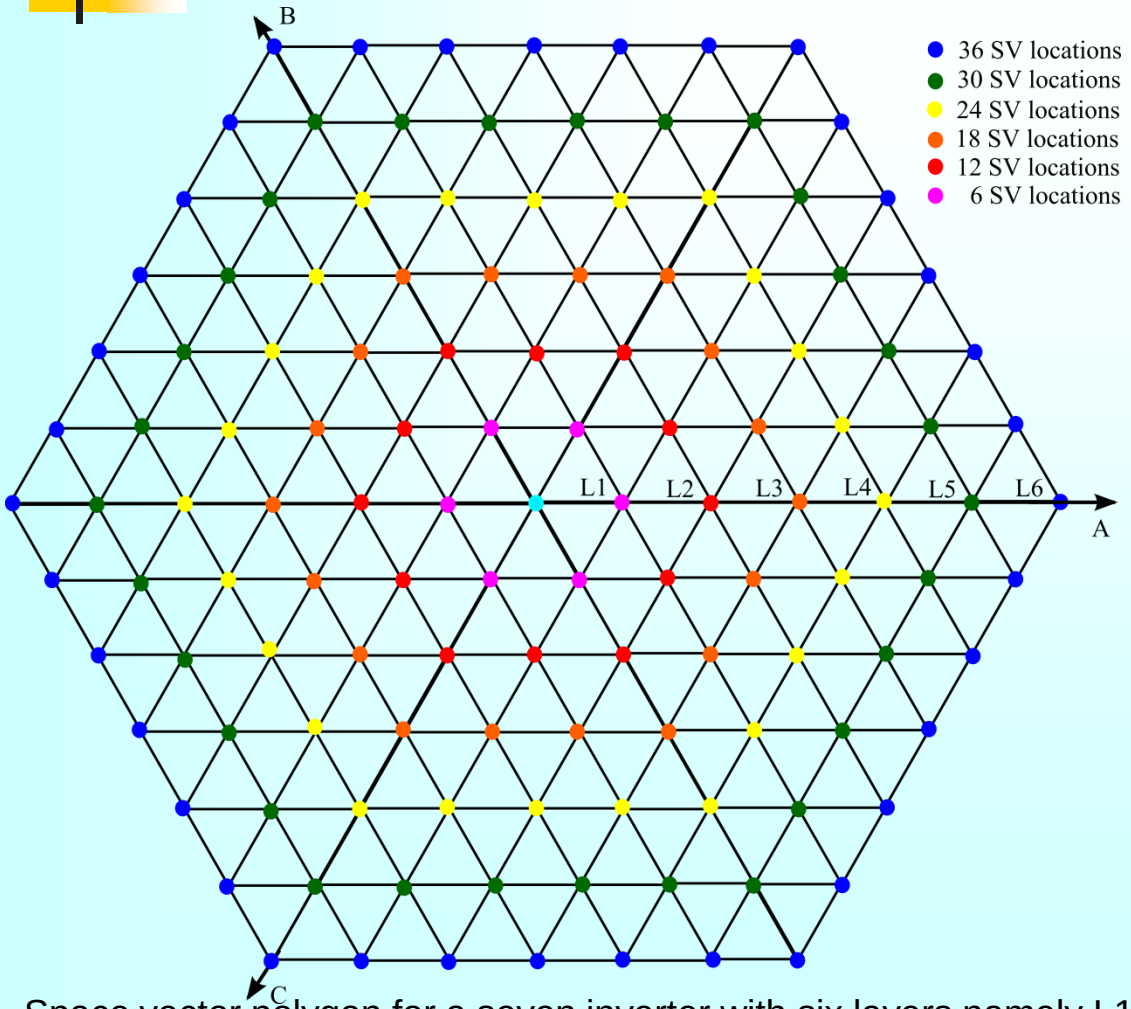


Generation of pole voltage $-2V_{dc}/6$



Generation of pole voltage $-V_{dc}/6$

Seven level space vector polygon



Space vector polygon for a seven inverter with six layers namely L1, L2, L3, L4, L5, L6.

- The proposed topology has 343(7^3) pole voltage combinations.
- These pole voltage combinations give 127 space vector locations.

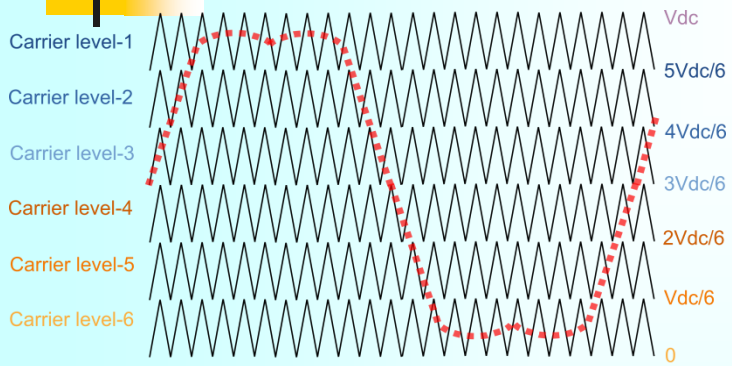
Salient features of proposed topology

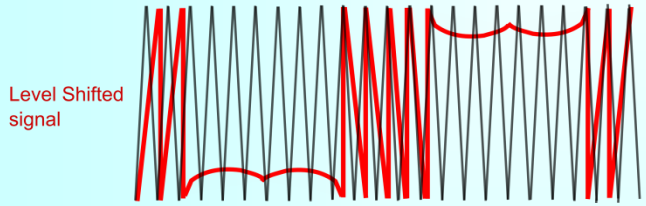
- Requires only single DC supply
- Less number of switching devices
- Capacitor voltages can be balanced over a switching cycle

Comparison of proposed inverter topology with other seven level topologies

Inverter Topology	Capacitor ($V_{dc}/6$)	IGBT			Clamping Diodes	Power supplies			
		$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$		V_{dc}	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$
Proposed Topology	18	12	6	12	0	1	0	0	0
NPC	6	0	0	36	90	1	0	0	0
FC	45	0	0	36	0	1	0	0	0
CHB	0	0	0	36	0	0			9

Level shifted carrier based PWM algorithm





- PWM signals are generated using level shifted carrier based PWM method

Experiment specifications

- Synchronous PWM technique is implemented for inverter operation above 10Hz
- Motor control algorithm - open-loop V/f control scheme
- IGBT module - SKM75GB123D
- DSP module - TMS320F28335
- FPGA module - SPARTAN-3-XC3S200
- Induction motor specification:

  3. 7 kW, 400 V, 50 Hz, 4-pole

  Stator resistance = 2.08Ω

  Rotor Resistance = 4.19Ω

  Stator Self inductance = 0.28H

  Rotor self inductance = 0.28H

  Magnetizing inductance = 0.272H

Frequency range	No. of samples/cycle
<10Hz	Asynchronous PWM,(f_{sw}=900Hz)
10 Hz-25 Hz	72
25Hz-37.5 Hz	48
37.5 Hz-48.85 Hz	36
48.85-50 Hz	6

Capacitor sizing

- The capacitor sizing is done by using the relation,

$$C = \frac{I_p}{f_s * \Delta V}$$

where,

I_p = **peak capacitor current (10A)**

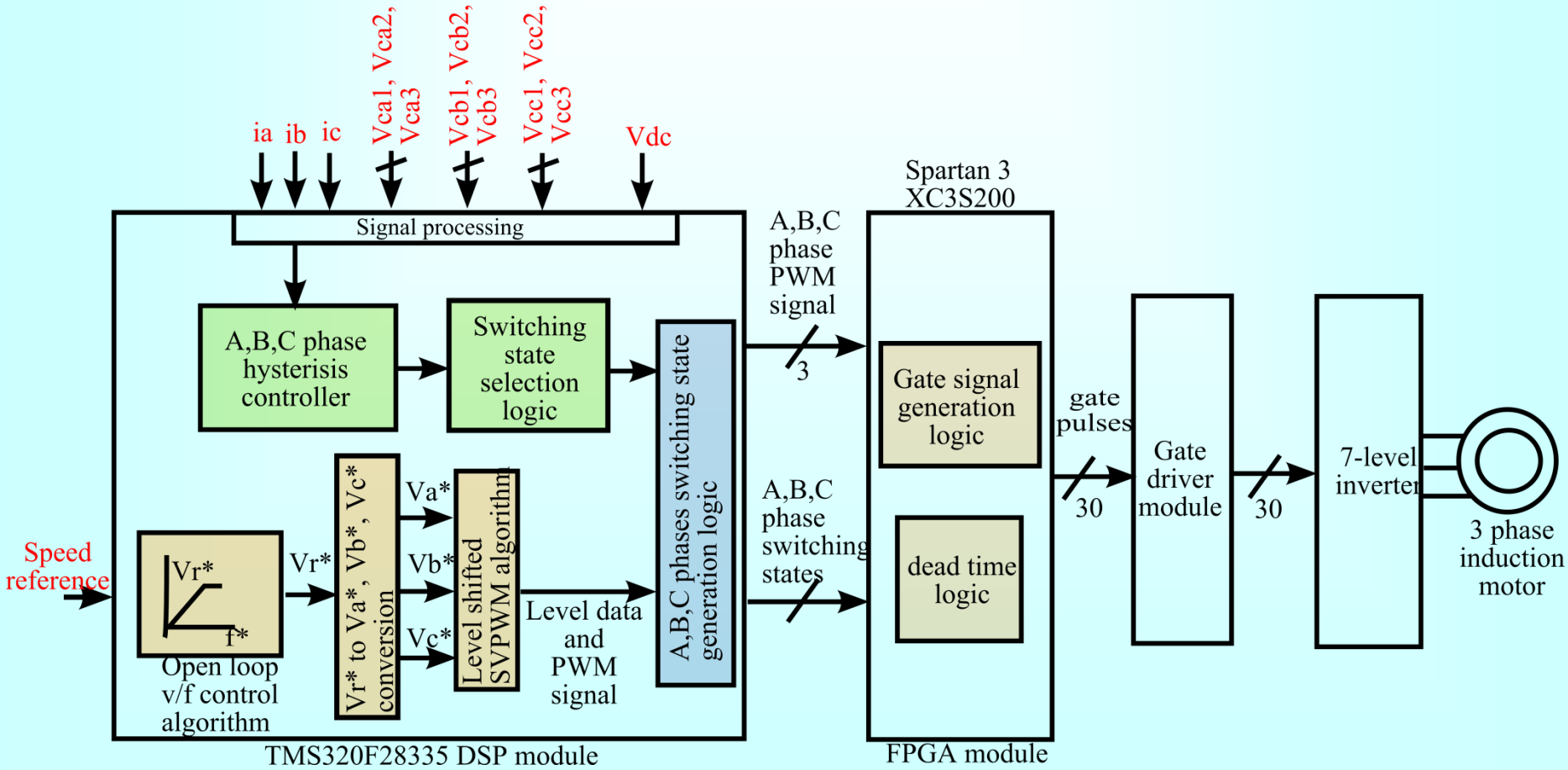
f_s = **minimum sampling frequency (1800Hz)**

ΔV = **peak to peak capacitor voltage ripple (2.5V)**

- For conducting the experiment, the capacitance value is selected as 2200 µF for all the three phases

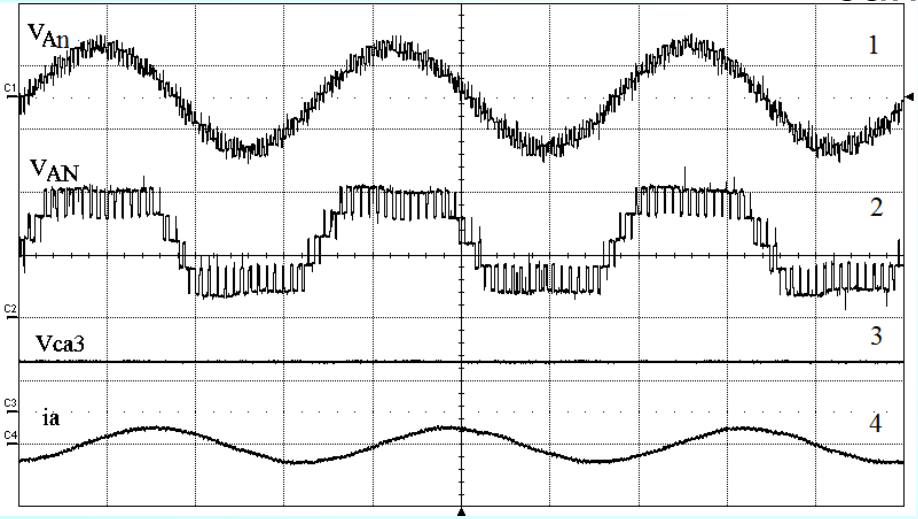
Implementation block diagram

- FPGA module is used as the PWM signal generator with dead time of 2. 5 us.

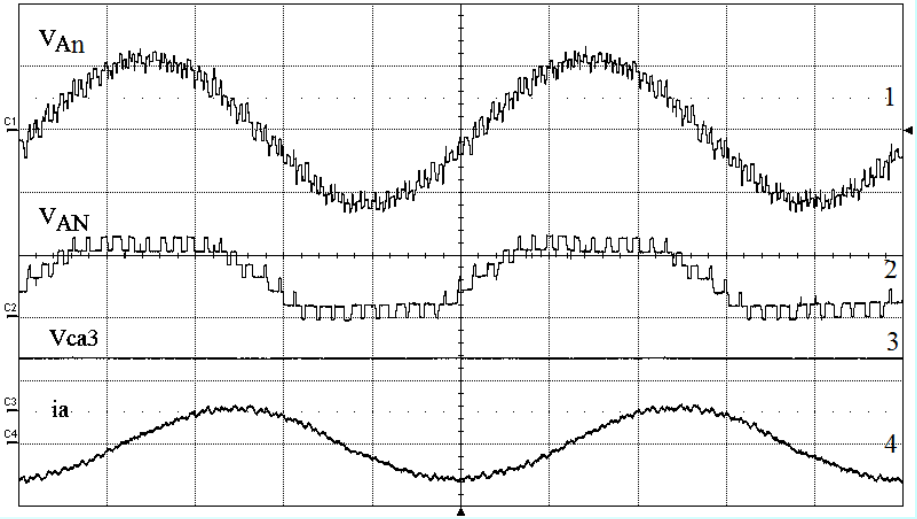


Experimental Results for steady state operation

- Motor phase voltage, inverter pole voltage, capacitor voltage and motor current



(a) 30Hz (MI=0.6), x-axis: 10ms/div

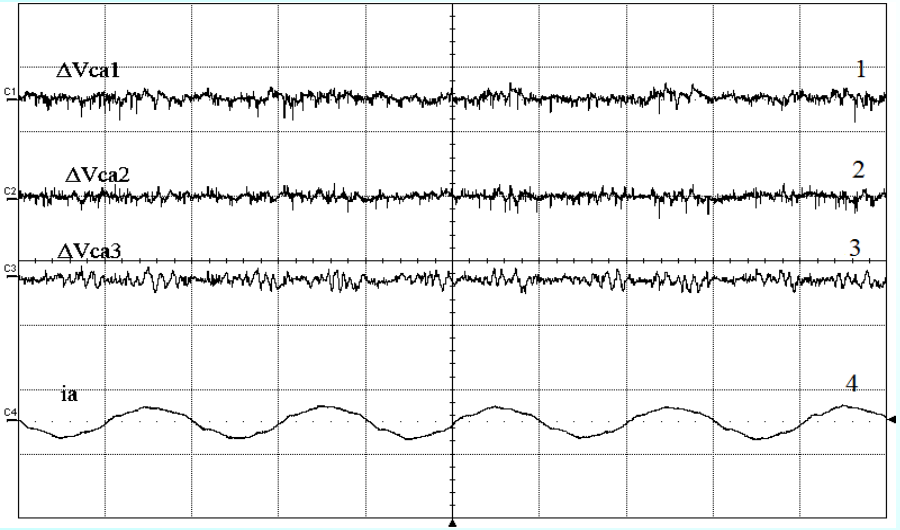


(b) 40Hz (MI=0.8), x-axis: 5ms/div

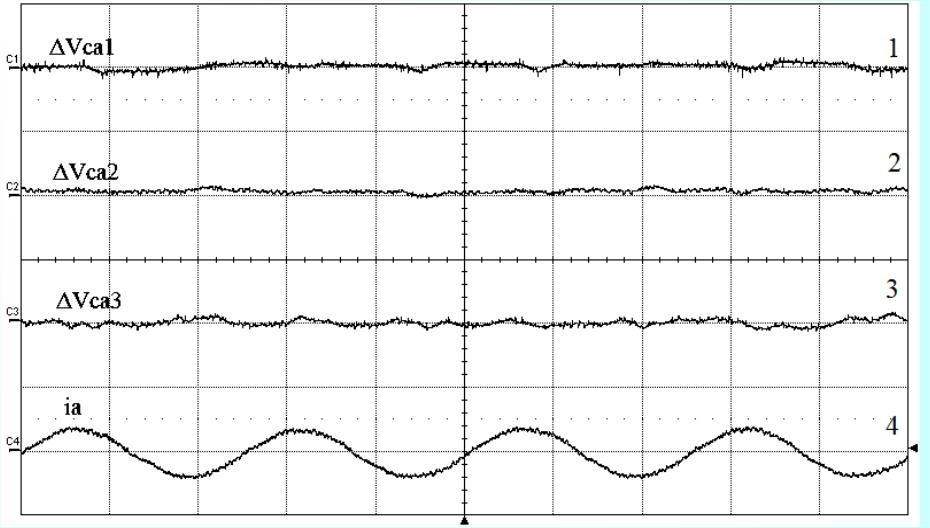
y-axis: 1) Motor Phase voltage (V_{An}) :200V/div, 2) Inverter Pole voltage (V_{AN}): 200V/div, 3) $V_{dc}/6$ Capacitor voltage (V_{ca3}): 50V/div, 4) Phase current (I_a): 2A/div.

Experimental Results for steady state operation

- Capacitor voltage ripple and motor phase current



(a) 10Hz (MI=0.2), x-axis: 50ms/div

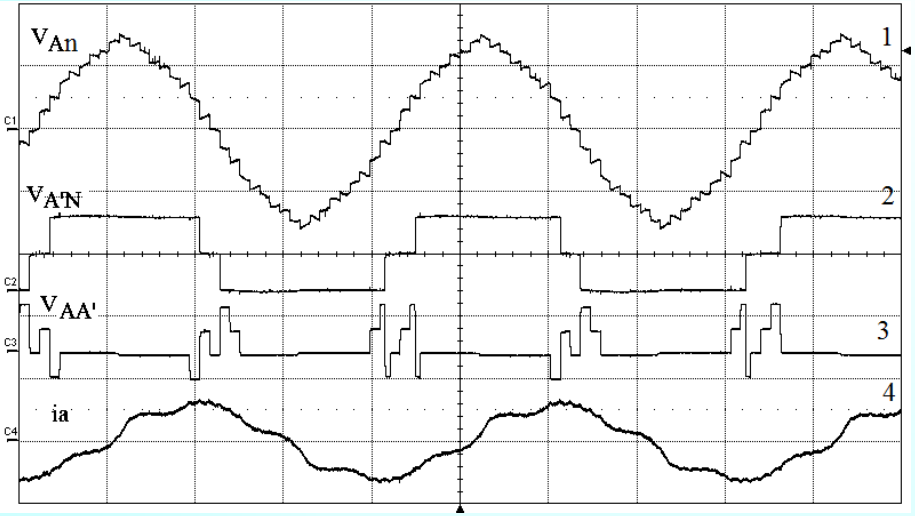


(b) 40Hz (MI=0.8), x-axis: 10ms/div

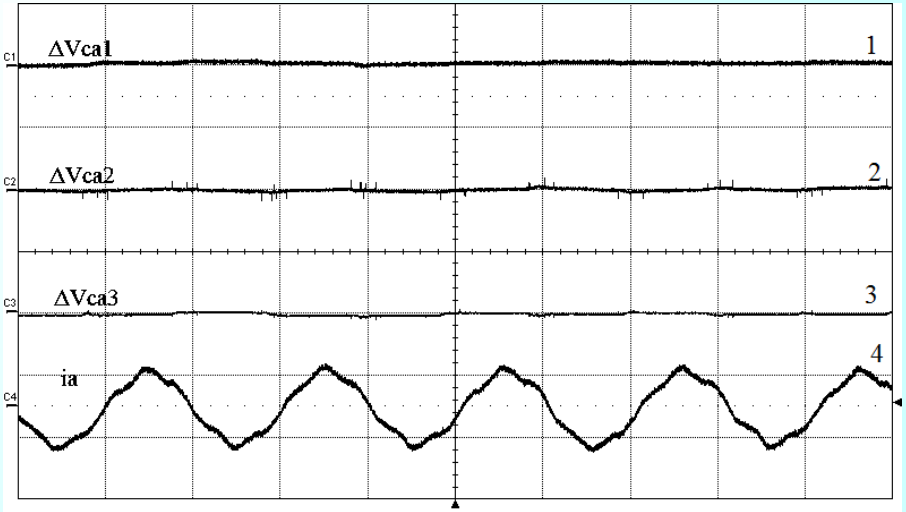
y-axis: 1) $V_{dc}/2$ capacitor voltage ripple(ΔVca1):2V/div, 2) $V_{dc}/3$ capacitor voltage ripple (ΔVca2): 2V/div, 3) $V_{dc}/6$ capacitor voltage ripple(ΔVca3): 2V/div,4) Phase current (I_a):2A/div

Experimental Results for steady state operation- Over modulation operation

- Tracing all the space vector locations of outer hexagon at frequency 48 Hz for phase ‘A’.



(a) 48Hz, x-axis-5ms/div

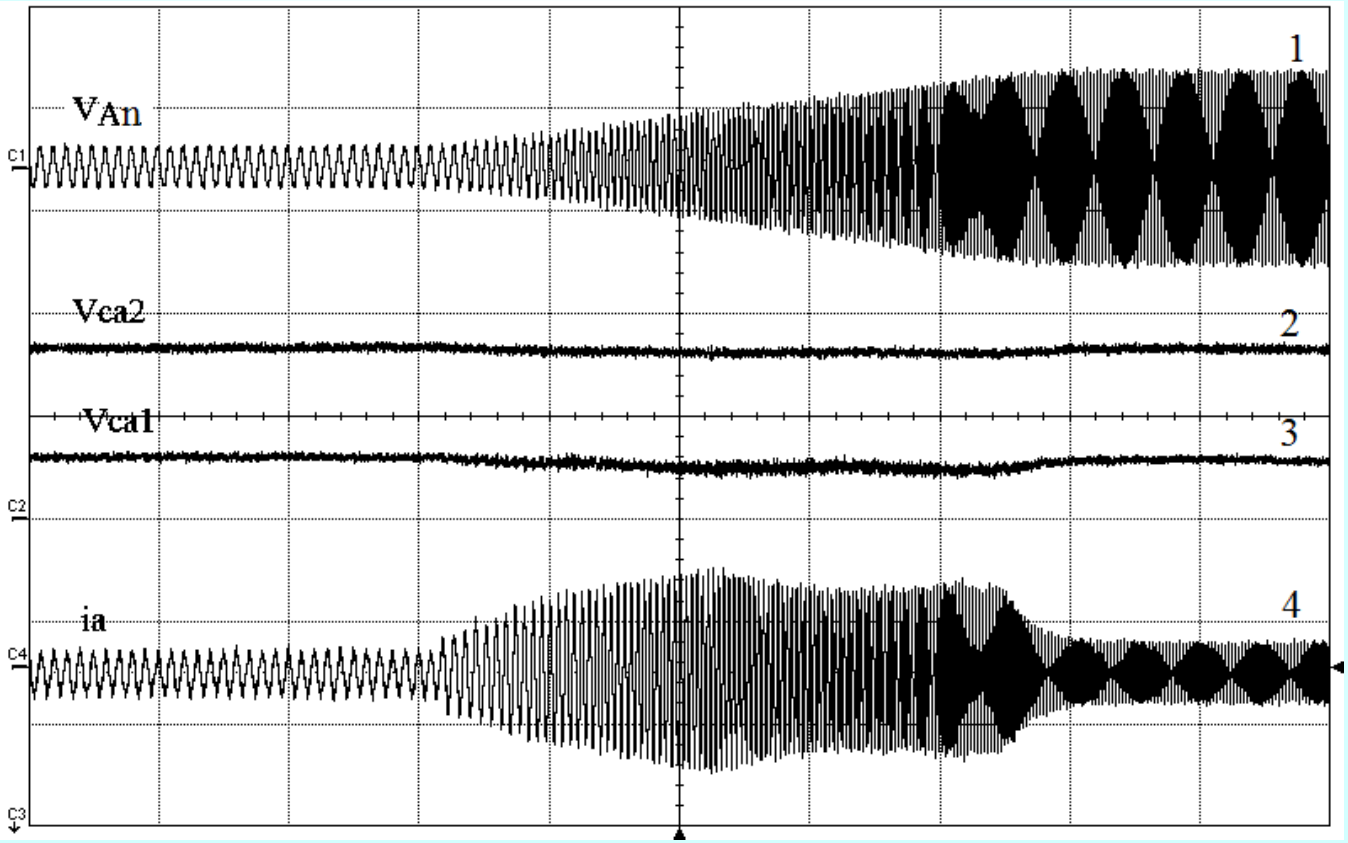


(b) 48Hz, x axis: 10ms/div

y-axis: (a) 1)Phase voltage (V_{An}:100V/div), 2) First flying capacitor pole voltage($V_{A'N}$: 100V/div), 3) Second flying capacitor pole voltage($V_{AA'}$:100V/div),3) Phase current (I_a:2A/div)
(b) 1) $V_{dc}/2$ capacitor voltage ripple(ΔVca1):2V/div, 2) $V_{dc}/3$ capacitor voltage ripple (ΔVca2): 2V/div, 3) $V_{dc}/6$ capacitor voltage ripple(ΔVca3): 2V/div,4) Phase current (I_a):2A/div

Experimental Results of acceleration of motor

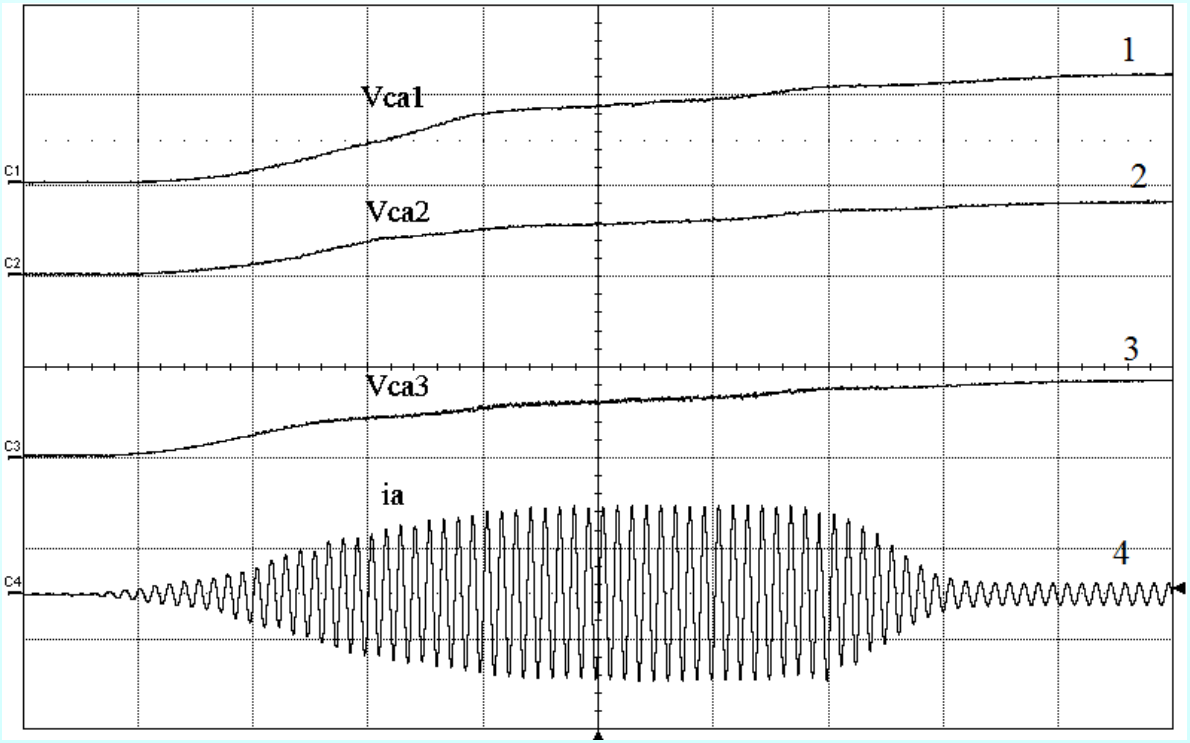
- Sudden acceleration of motor from 10Hz to 40 Hz in 4s



x-axis: 1s/div, y-axis: 1) Phase voltage (V_{An}): 200 V/div, 2) V_{dc}/2 capacitor voltage (Vca1): 50V/div, 3) V_{dc}/3 capacitor DC voltage (Vca2): 20V/div, 4) Phase current (I_a):2A/div

Experimental Results - starting transients

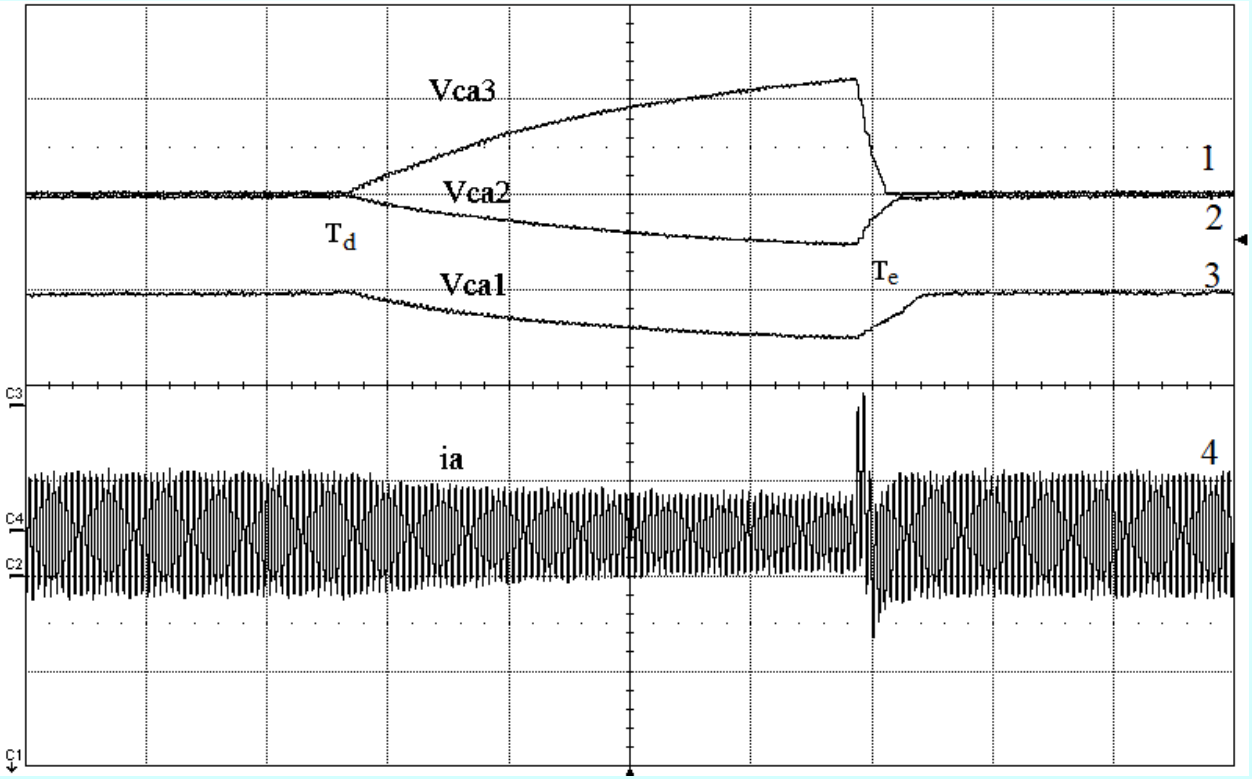
- Charging of capacitor voltages to the reference voltage for phase 'A' when inverter is switched on



x-axis: 200ms/div, y-axis Y-axis: 1) $V_{dc}/2$ capacitor voltage ripple(ΔVca1):2V/div, 2) $V_{dc}/3$ capacitor voltage ripple (ΔVca2): 2V/div, 3) $V_{dc}/6$ capacitor voltage ripple(ΔVca3): 2V/div,4) Phase current (I_a):5A/div

Experimental Results- capacitor voltage balancing algorithm testing

- Capacitor voltage balancing is disabled at T_d and again enabled at T_e for A phase at 40Hz



x-axis: 500ms/div, y-axis Y-axis: 1) $V_{dc}/2$ capacitor voltage ripple(ΔVca1):2V/div, 2) $V_{dc}/3$ capacitor voltage ripple (ΔVca2): 2V/div, 3) $V_{dc}/6$ capacitor voltage ripple(ΔVca3): 2V/div,4) Phase current (I_a):5A/div.

Conclusion

- A new 3 phase seven level inverter topology is developed by cascading two flying capacitor three level inverter with a half bridge module and experimental results are presented.
- A hysteresis controller based capacitor voltage balancing scheme is implemented and tested for various frequencies.
- Capacitor voltage balancing for the proposed topology can be obtained irrespective of the load current power factor and direction.

The key advantages of proposed topology are

- Reduced number of switches
- Reduced capacitor sizing
- Single dc supply requirement and simple control.

Thank you