Reduced Switch Count Multilevel Inverter Topologies for Open End Induction Motor Drives

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Outline

Outline

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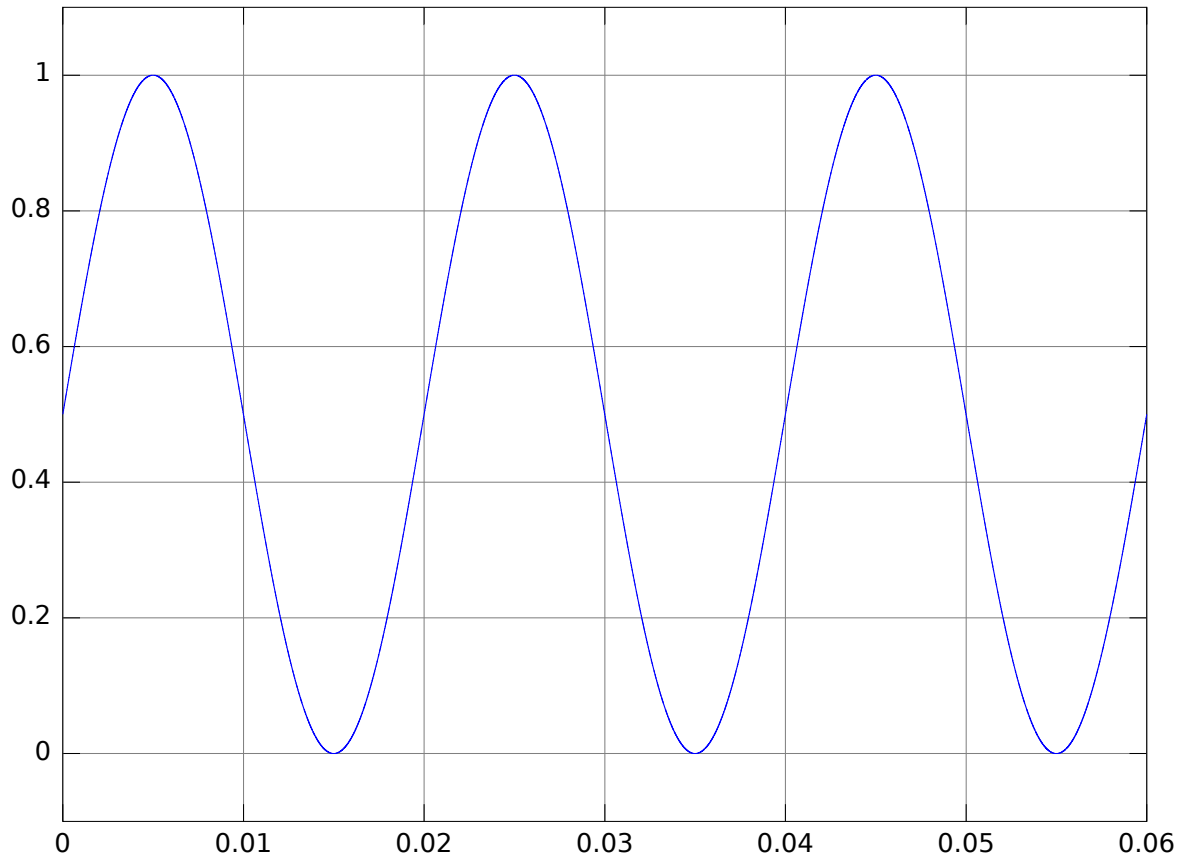
Introduction

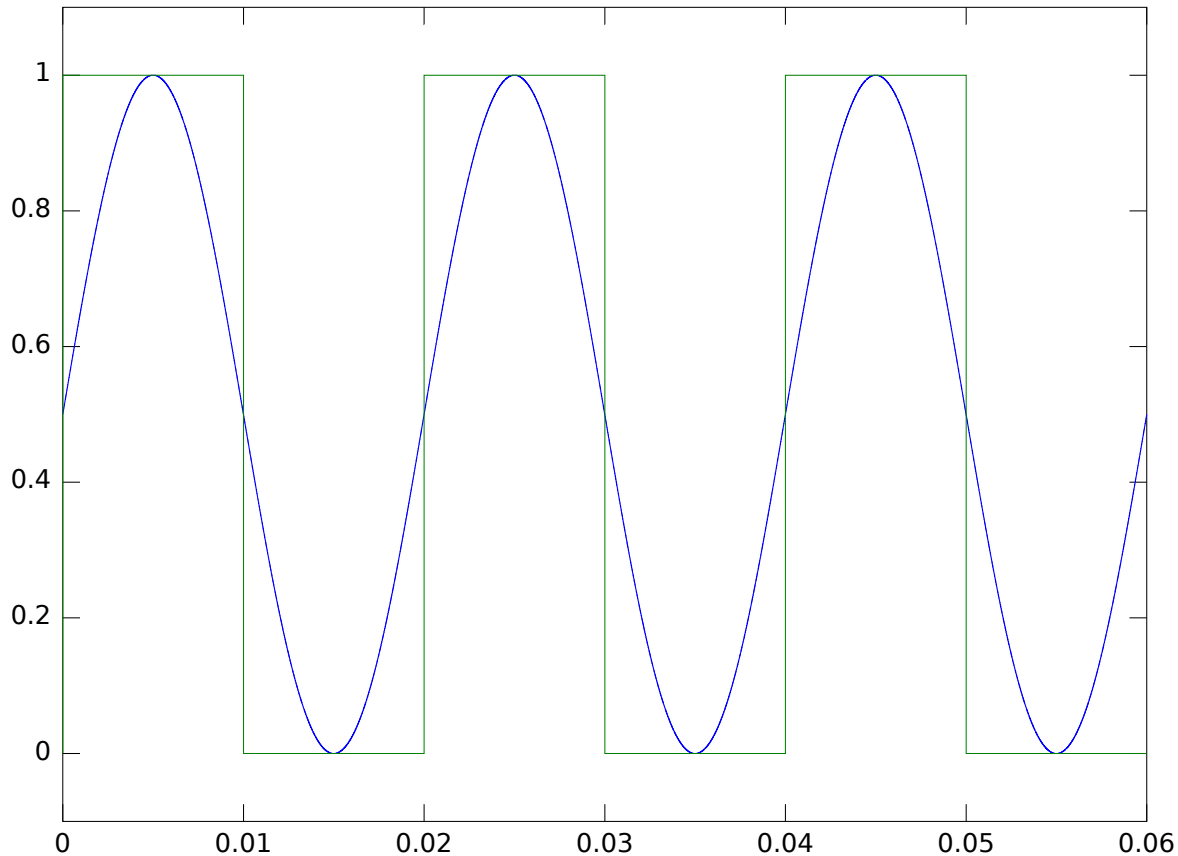
Why Inverters?

AC loads need sinusoidal voltage w/ controllable V,f



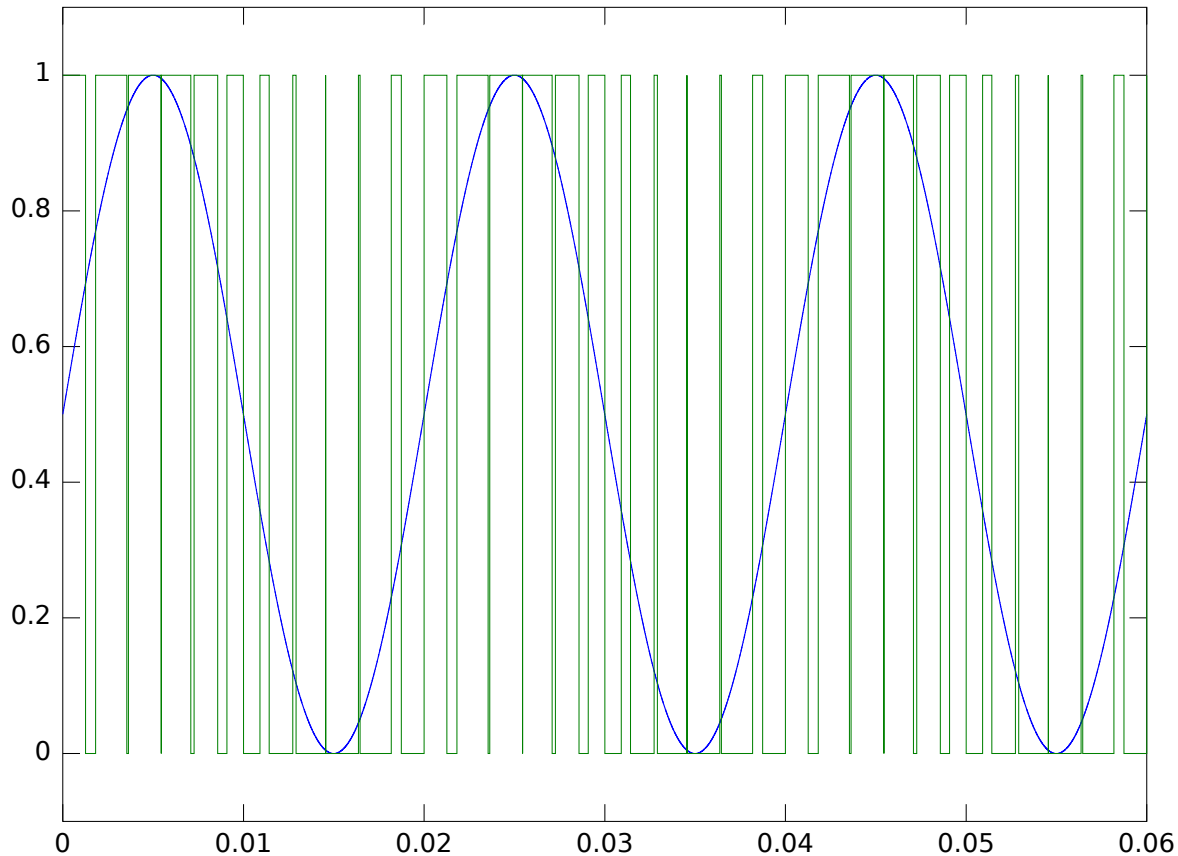
Two-Level inverters

Squarewave switching: low losses; bad harmonics



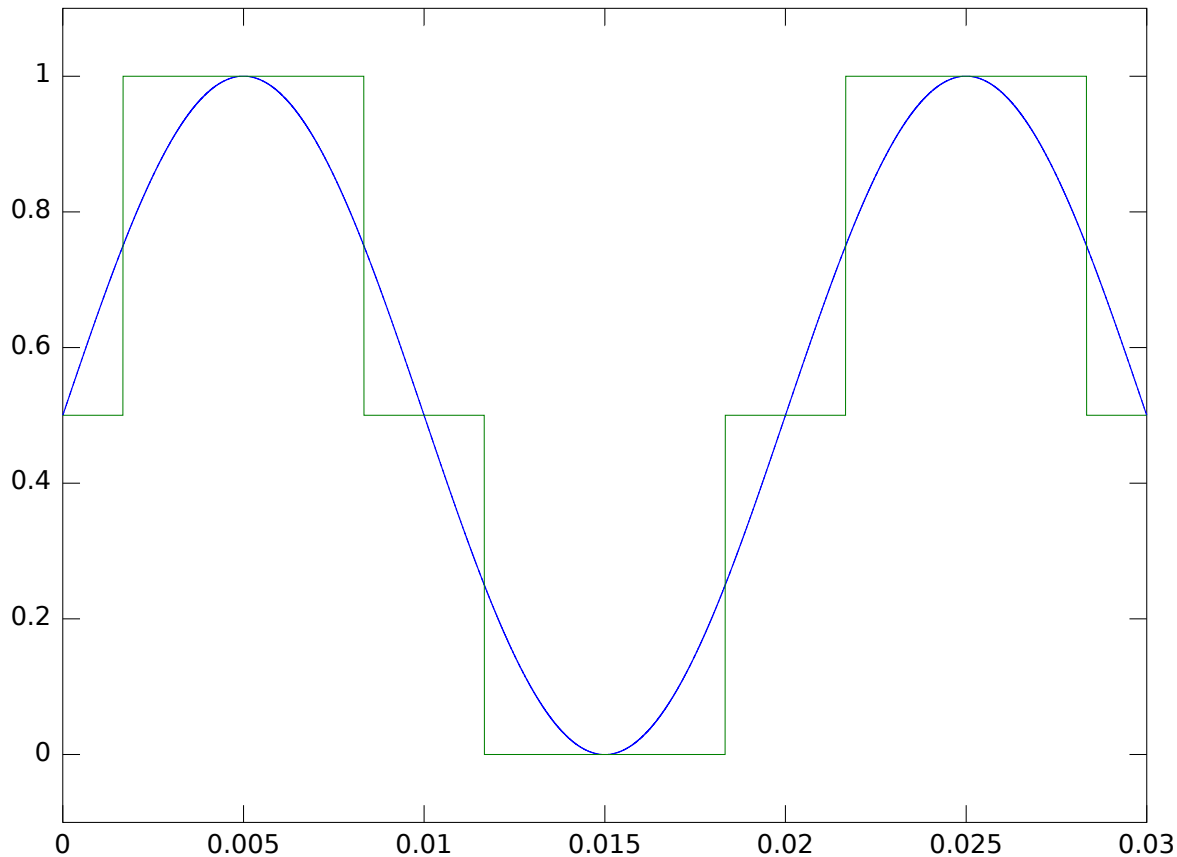
Two-Level inverters

PWM: more switching; better harmonics



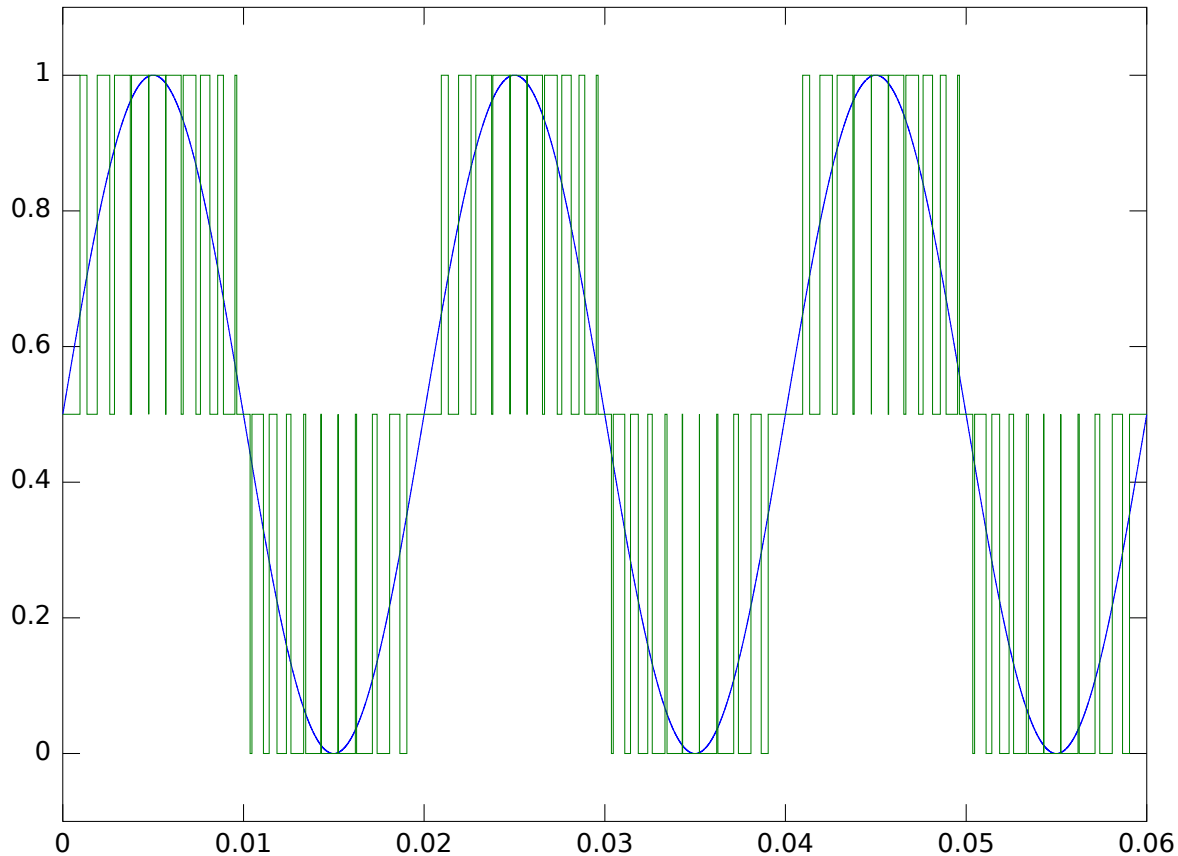
Three-level inverter

Stepped operation



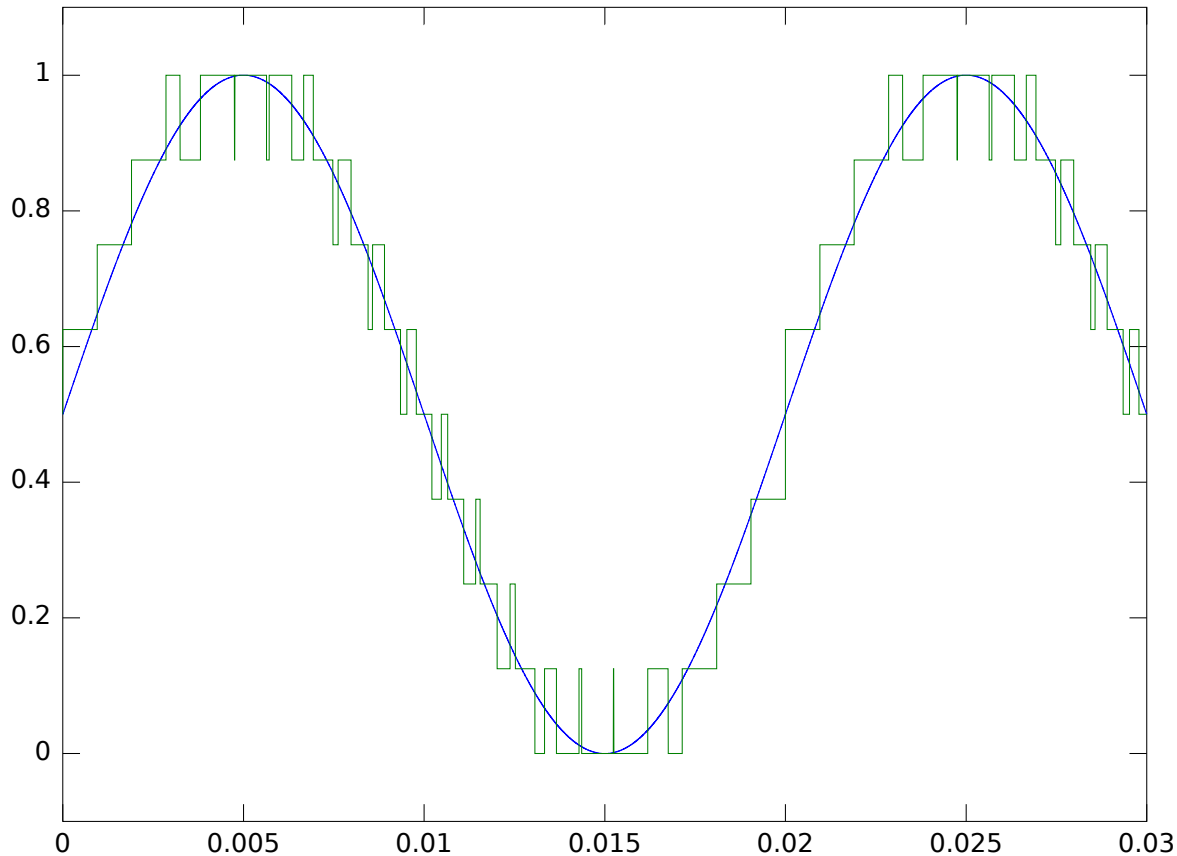
Three-level inverter

PWM Operation



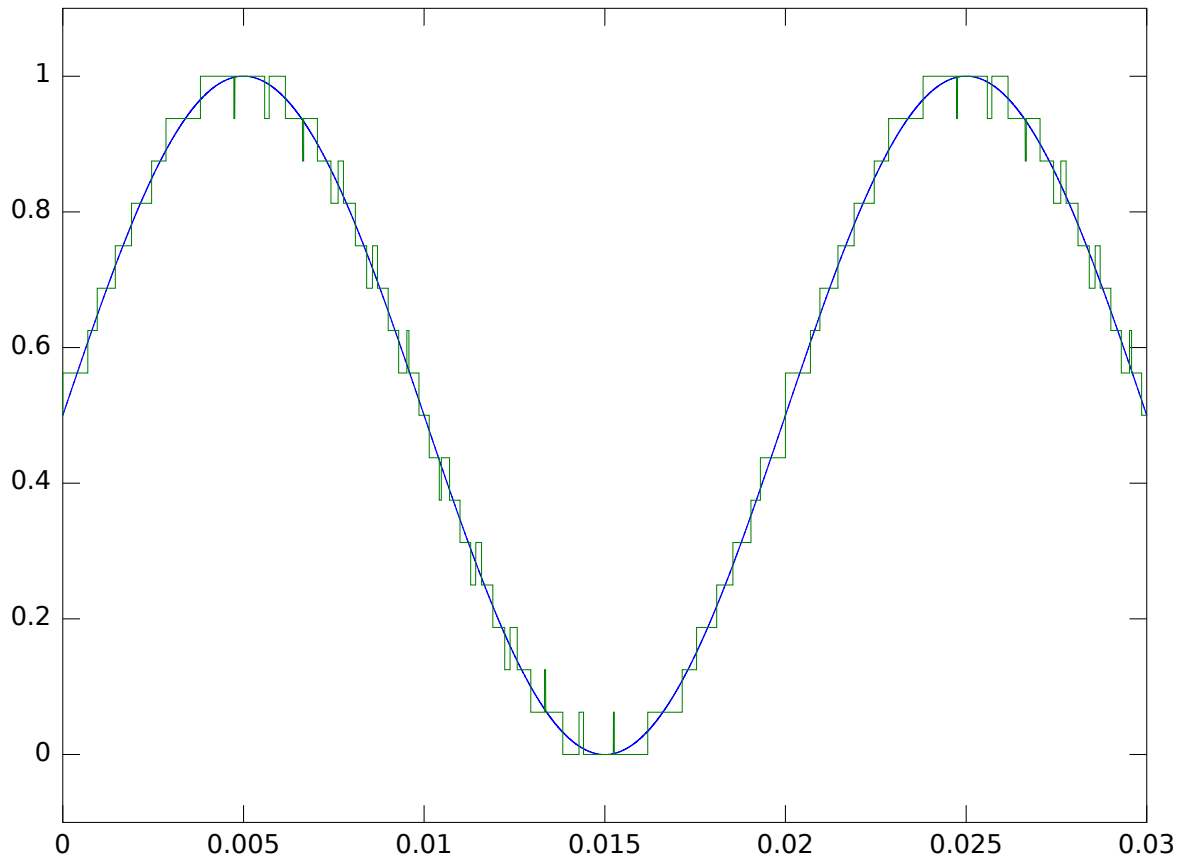
Nine-Level inverters

Great harmonics!



Seventeen-Level inverters

Phenomenal harmonics!

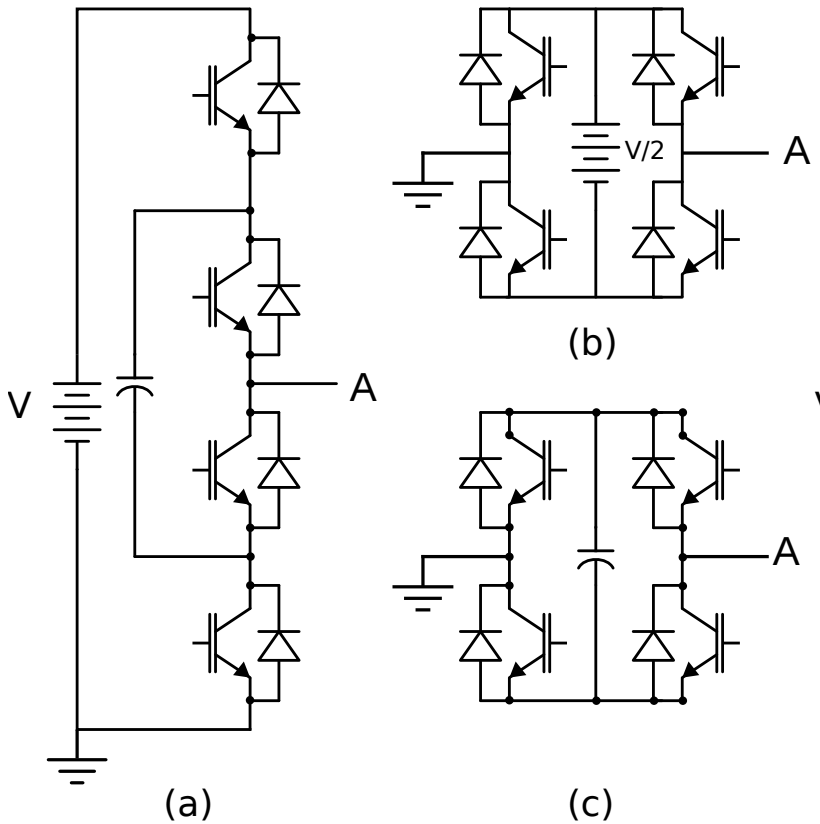


Multilevel converters

Advantages

- Lower dV/dt
- Lower harmonics
- Reduced torque ripple
- Improved EMI/EMC performance

Existing Multilevel Inverter Topologies



(a) Three level Flying Capacitor topology (one phase)

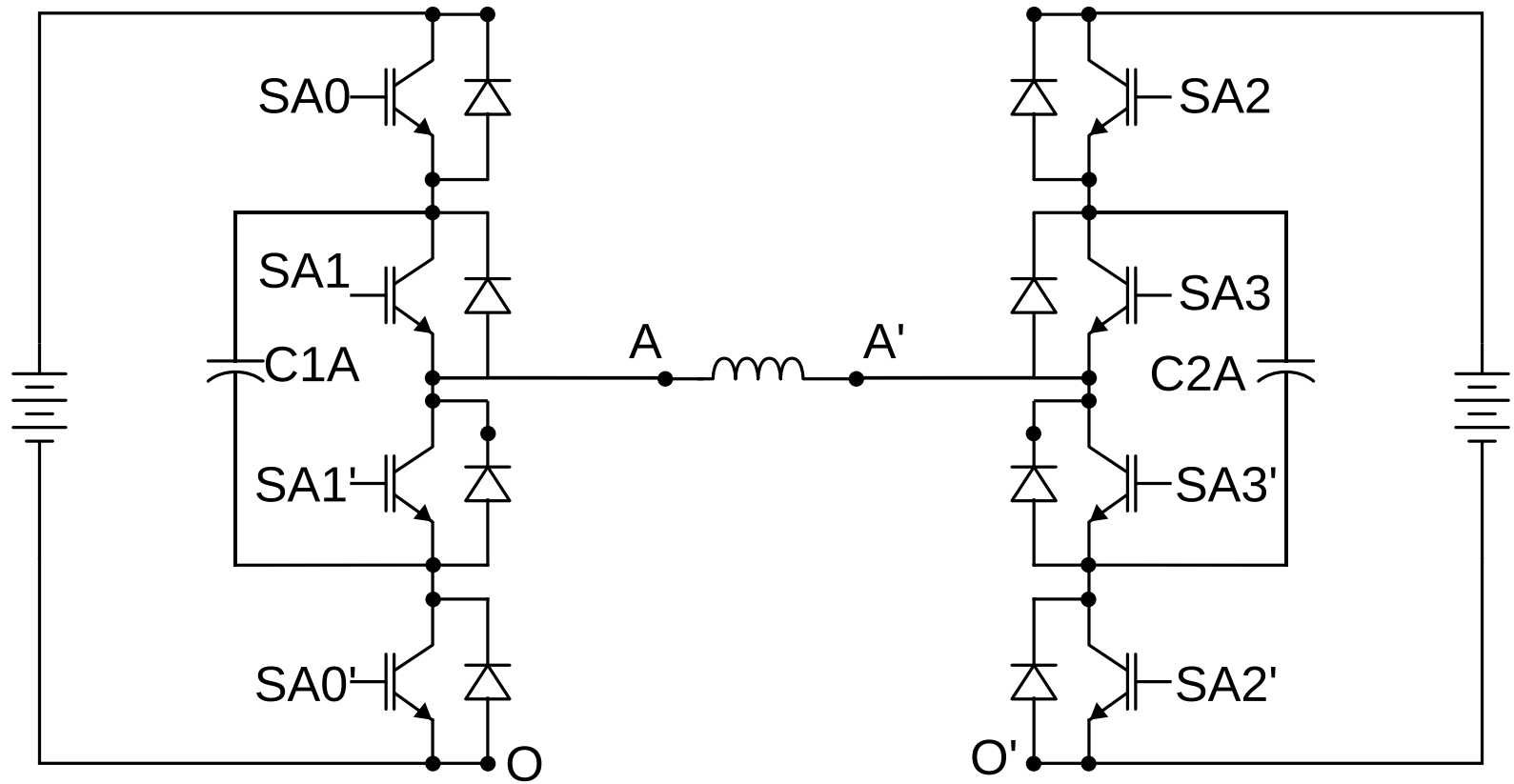
(b,c) Three level Cascaded H-Bridge Topology (one phase)

(d) Three level Neutral Point Clampded topology (one phase)

Nine Level Inverter Topology for Open End Induction Motor Drive

Circuit topology

Proposed Topology for Nine-Level Inverter (One phase shown)



Circuit topology

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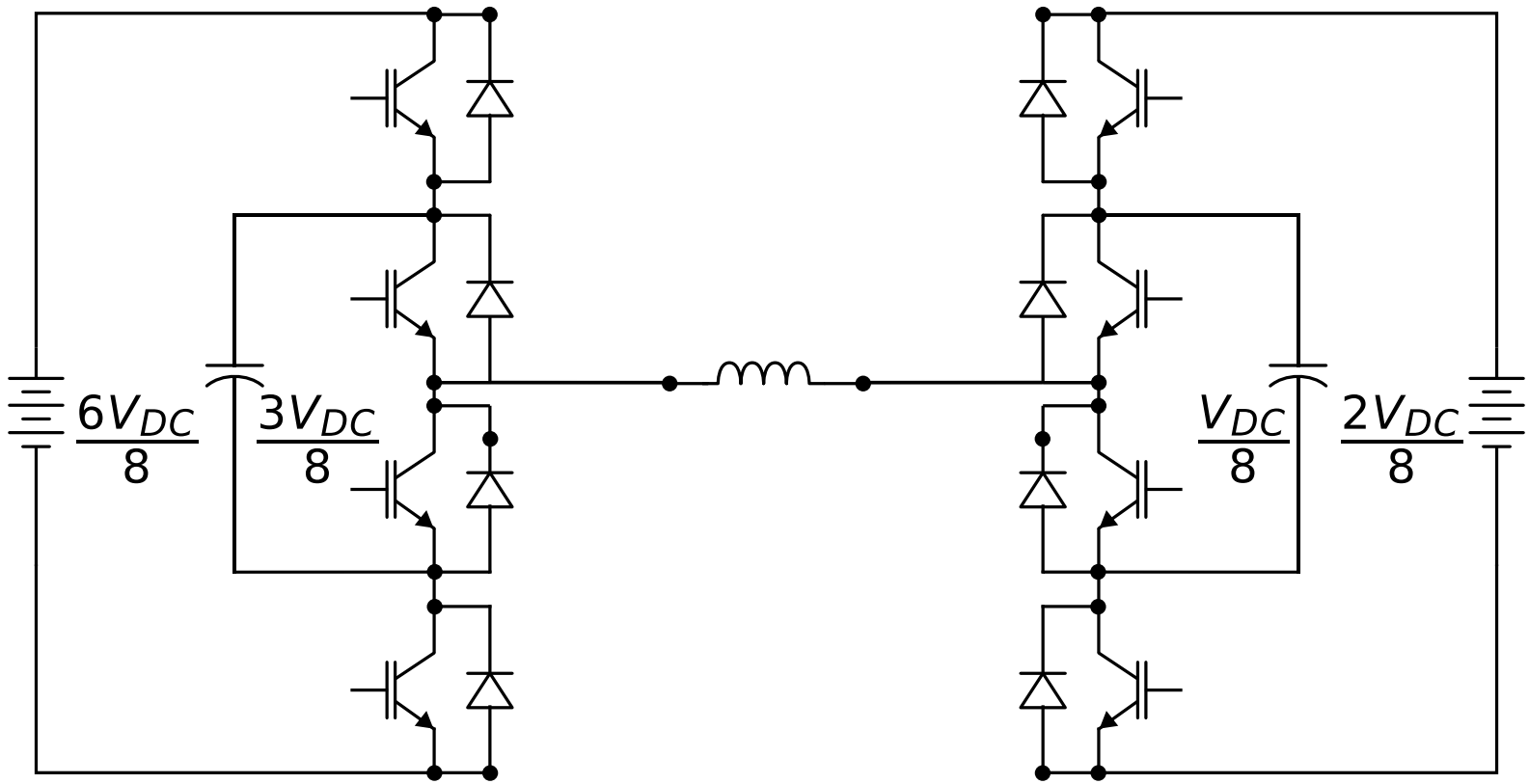
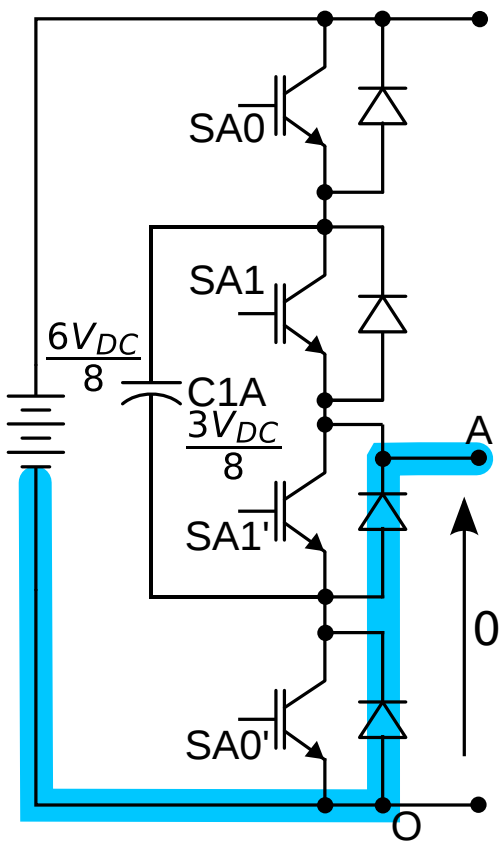
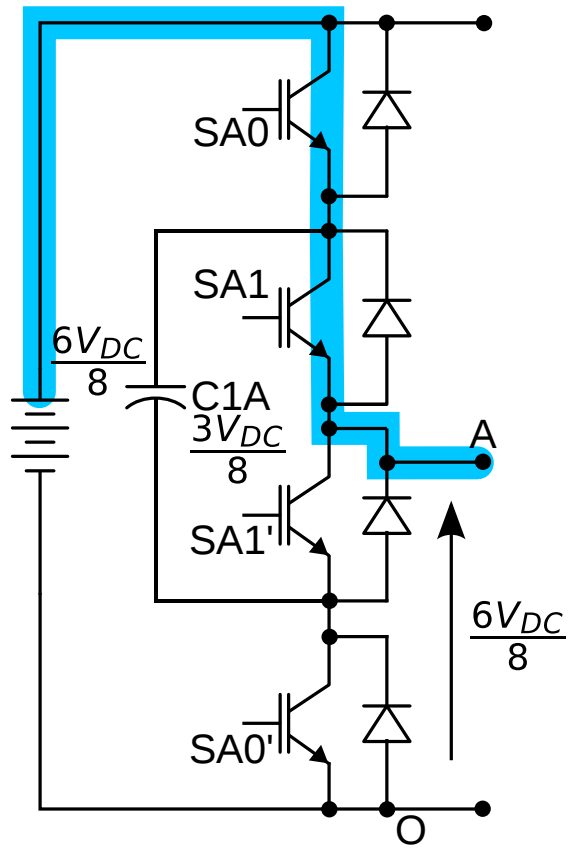
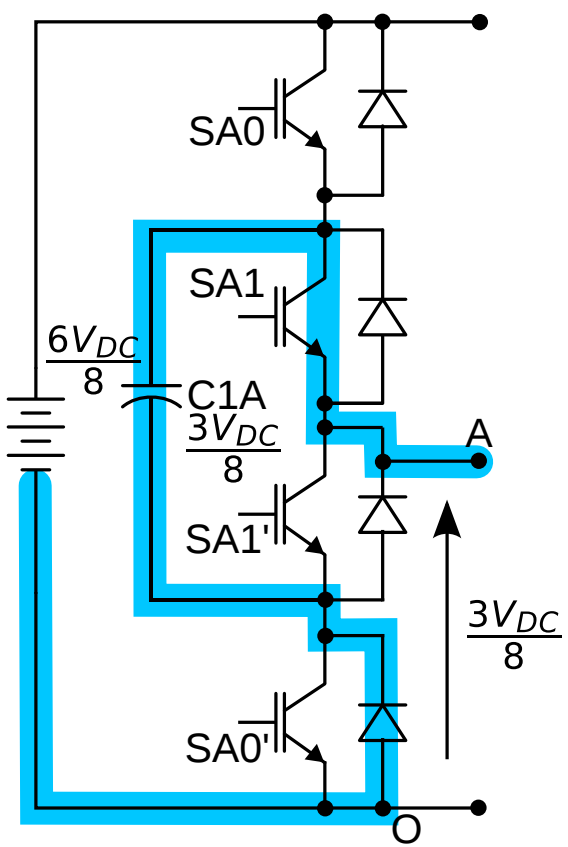


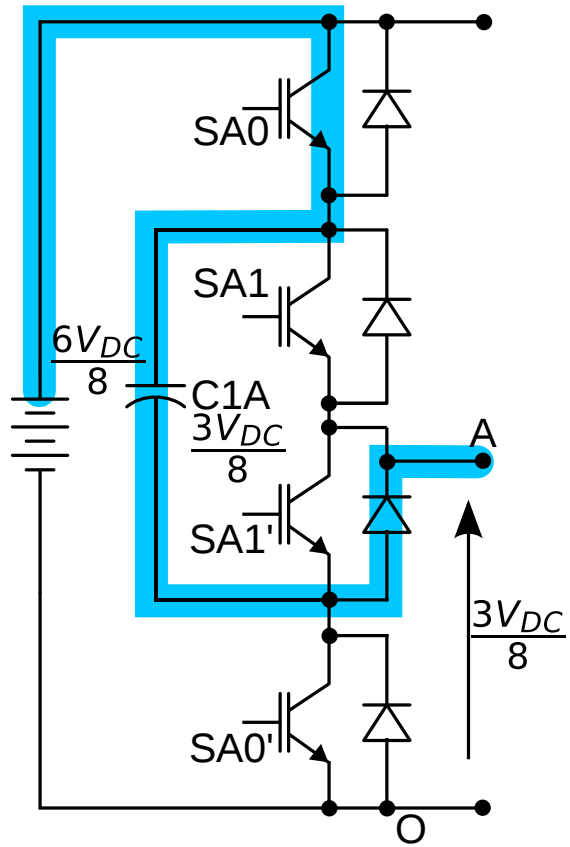
Pole Voltages of Inverter-1



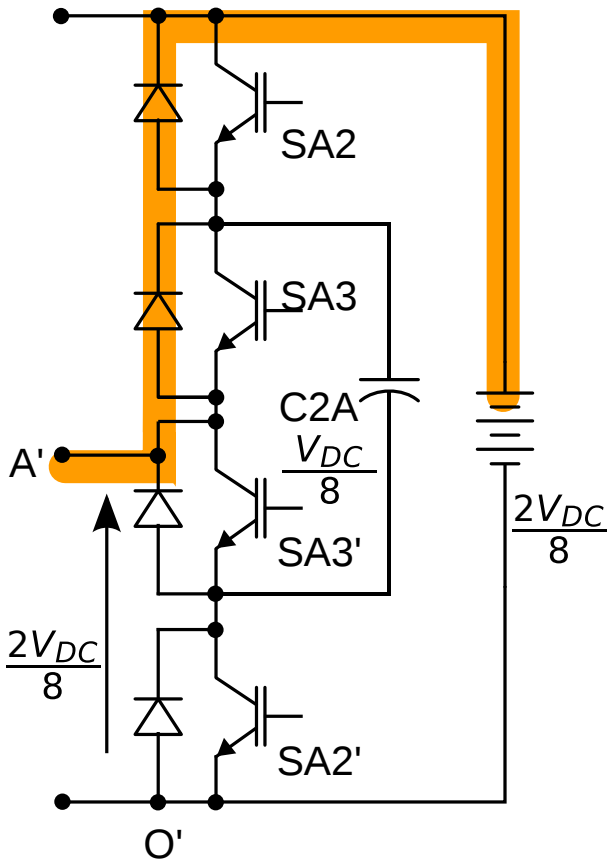


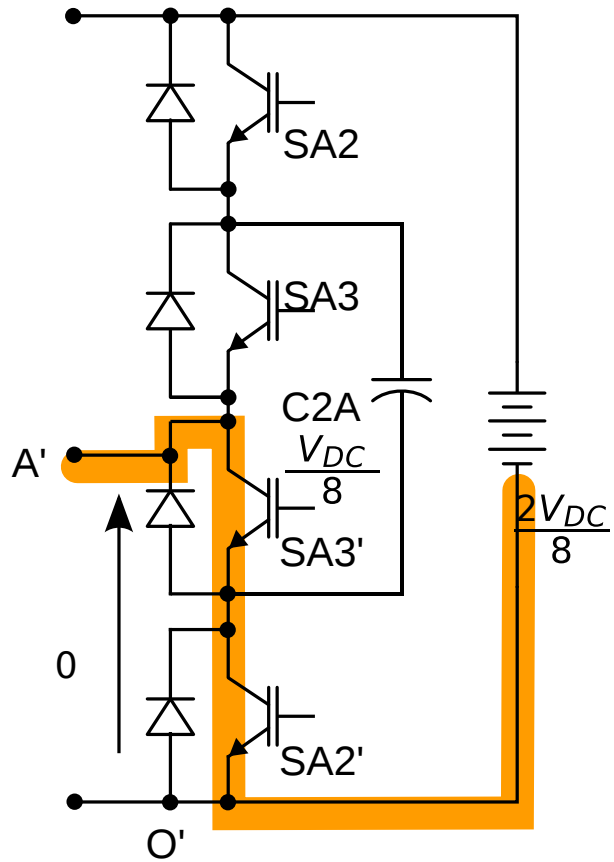
Pole Voltages of Inverter-1



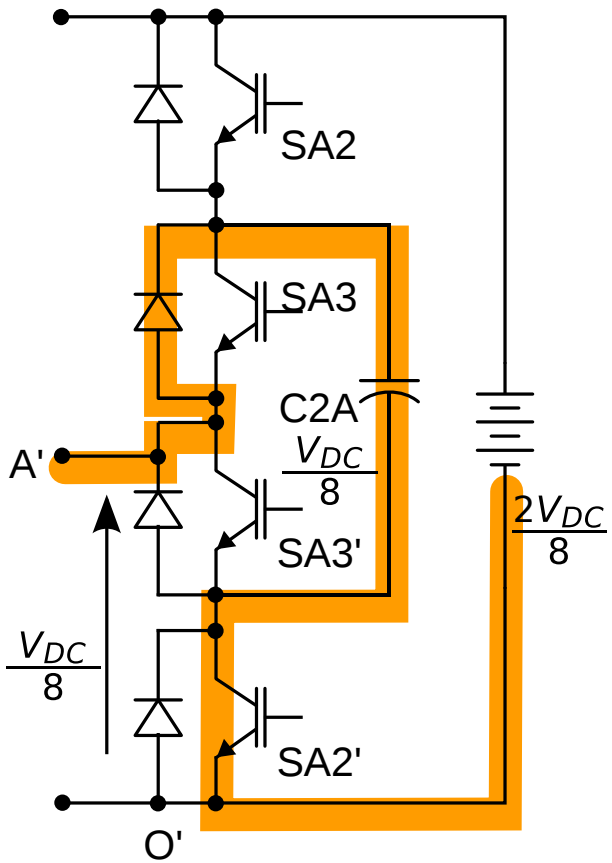


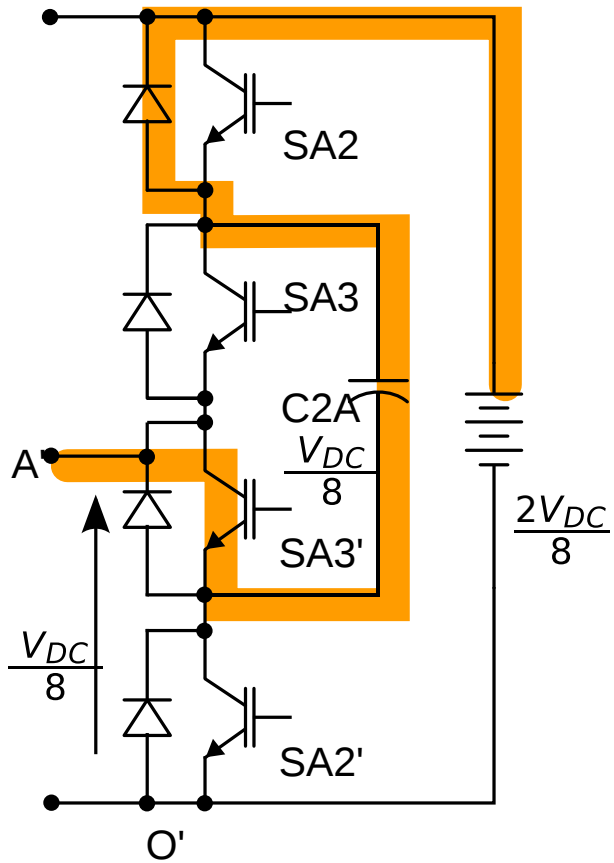
Pole Voltages of Inverter-2





Pole Voltages of Inverter-2





Pole Voltage Levels

Table: $V_{AA;}$ values for all possible combinations of V_{AO} and $V_{A'O'}$

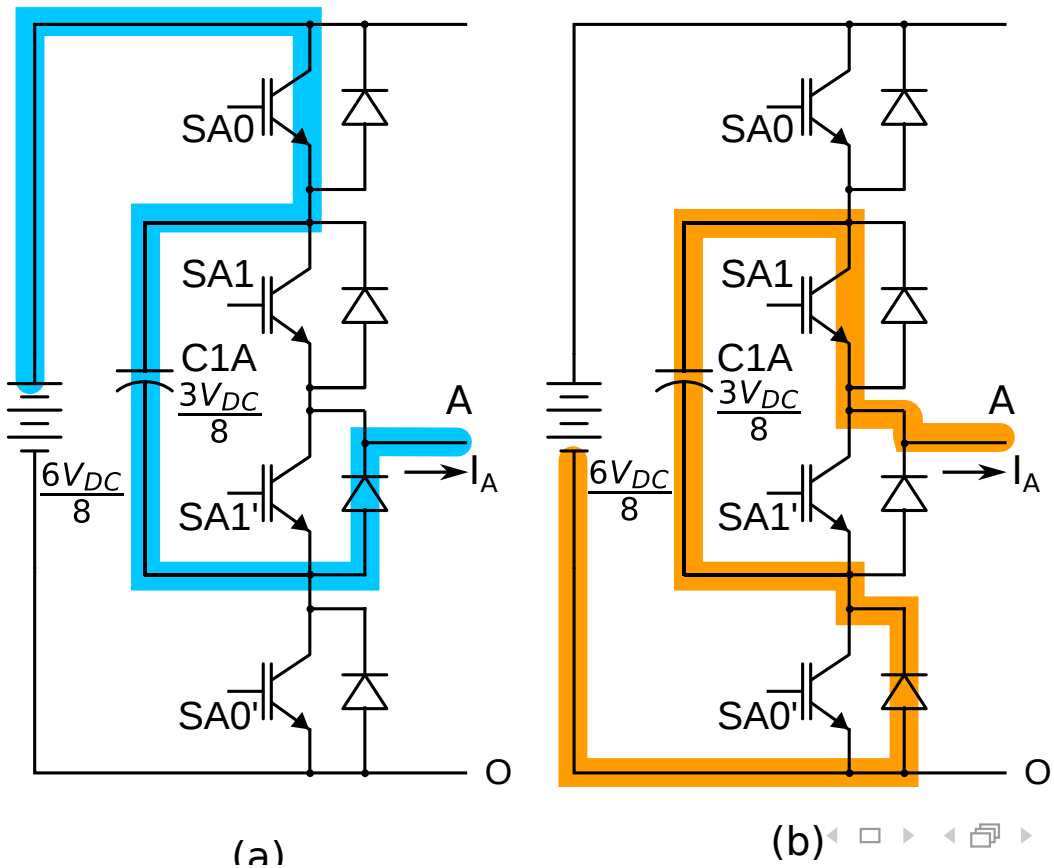
Level	$\mathbf{V_{AA'}}$	$\mathbf{V_{AO}}$	$\mathbf{V_{A'O'}}$
0	$-2V_{DC}/8$	0	$2V_{DC}/8$
1	$-V_{DC}/8$	0	$V_{DC}/8$
2	0	0	0
3	$V_{DC}/8$	$3V_{DC}/8$	$2V_{DC}/8$
4	$2V_{DC}/8$	$3V_{DC}/8$	$V_{DC}/8$
5	$3V_{DC}/8$	$3V_{DC}/8$	0
6	$4V_{DC}/8$	$6V_{DC}/8$	$2V_{DC}/8$
7	$5V_{DC}/8$	$6V_{DC}/8$	$V_{DC}/8$
8	$6V_{DC}/8$	$6V_{DC}/8$	0

Switching Redundancies for Capacitor Balancing

Switching states for Pole voltage $3V_{DC}$:

(a) C1A charging

(b) C1A discharging



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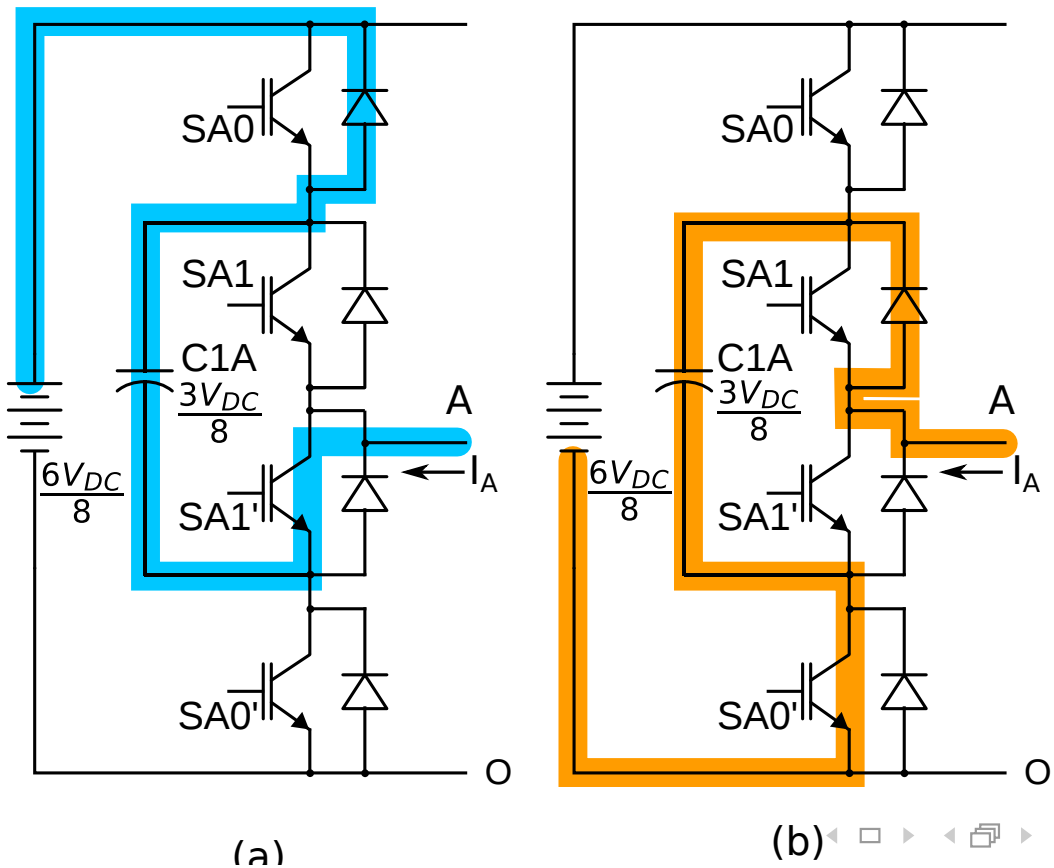
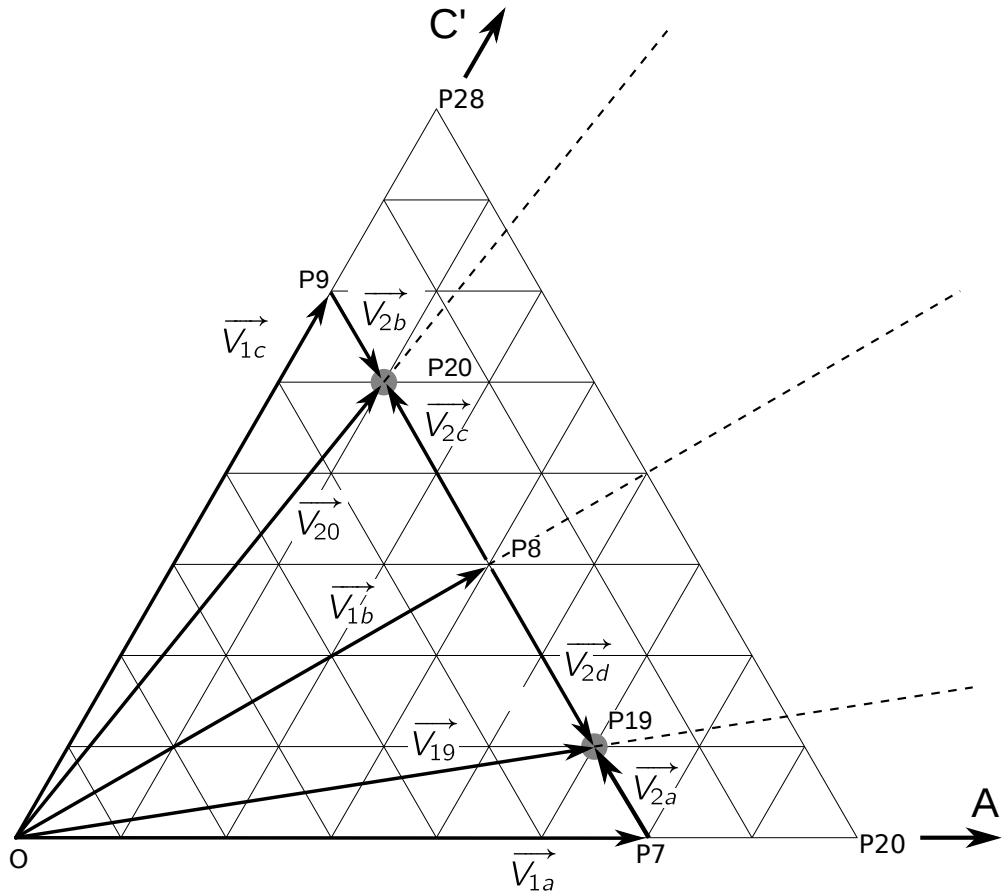


Instantaneous Capacitor Balancing

- Independent of current direction
- Independent of other phases
- No Precharging required
- Switching state choice updated every switching period
- Low capacitance requirement

Vector combinations

to ensure power supply from both inverters



- (P20): $\vec{V}_{20}$

$$= \vec{V}_{1c} + \vec{V}_{2b} \quad \text{(outer)}$$
$$= \vec{V}_{1b} + \vec{V}_{2c} \quad \text{(inner)}$$

- (P19): $\vec{V}_{19}$

$$= \vec{V}_{1a} + \vec{V}_{2a} \quad \text{(outer)}$$
$$= \vec{V}_{1b} + \vec{V}_{2d} \quad \text{(inner)}$$

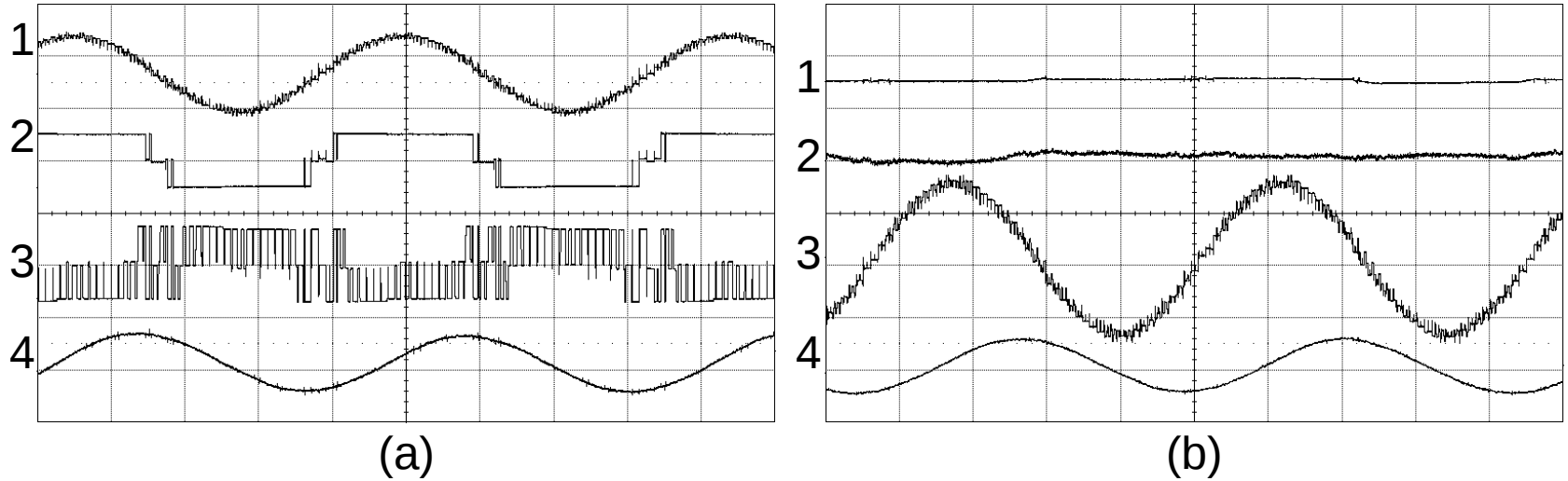
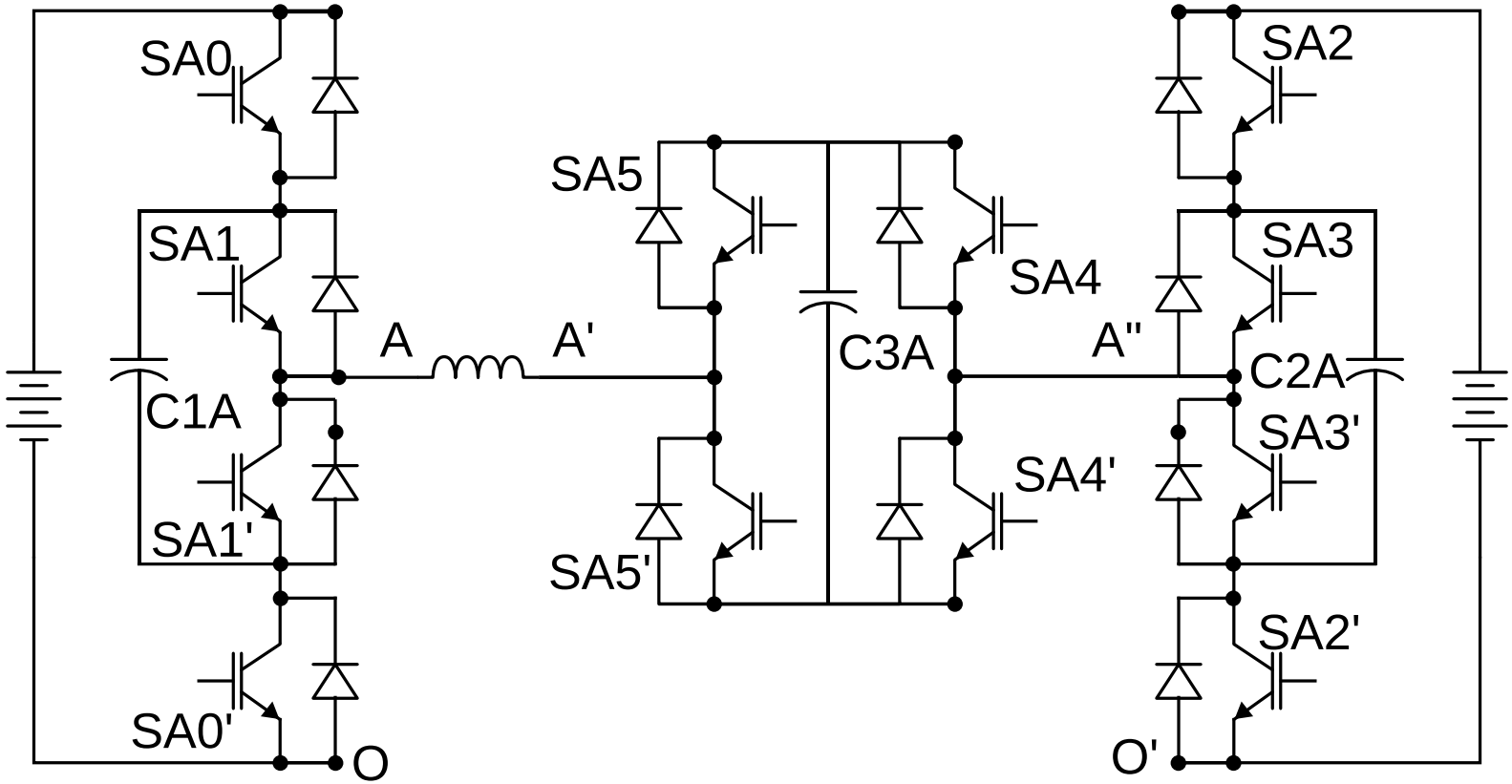


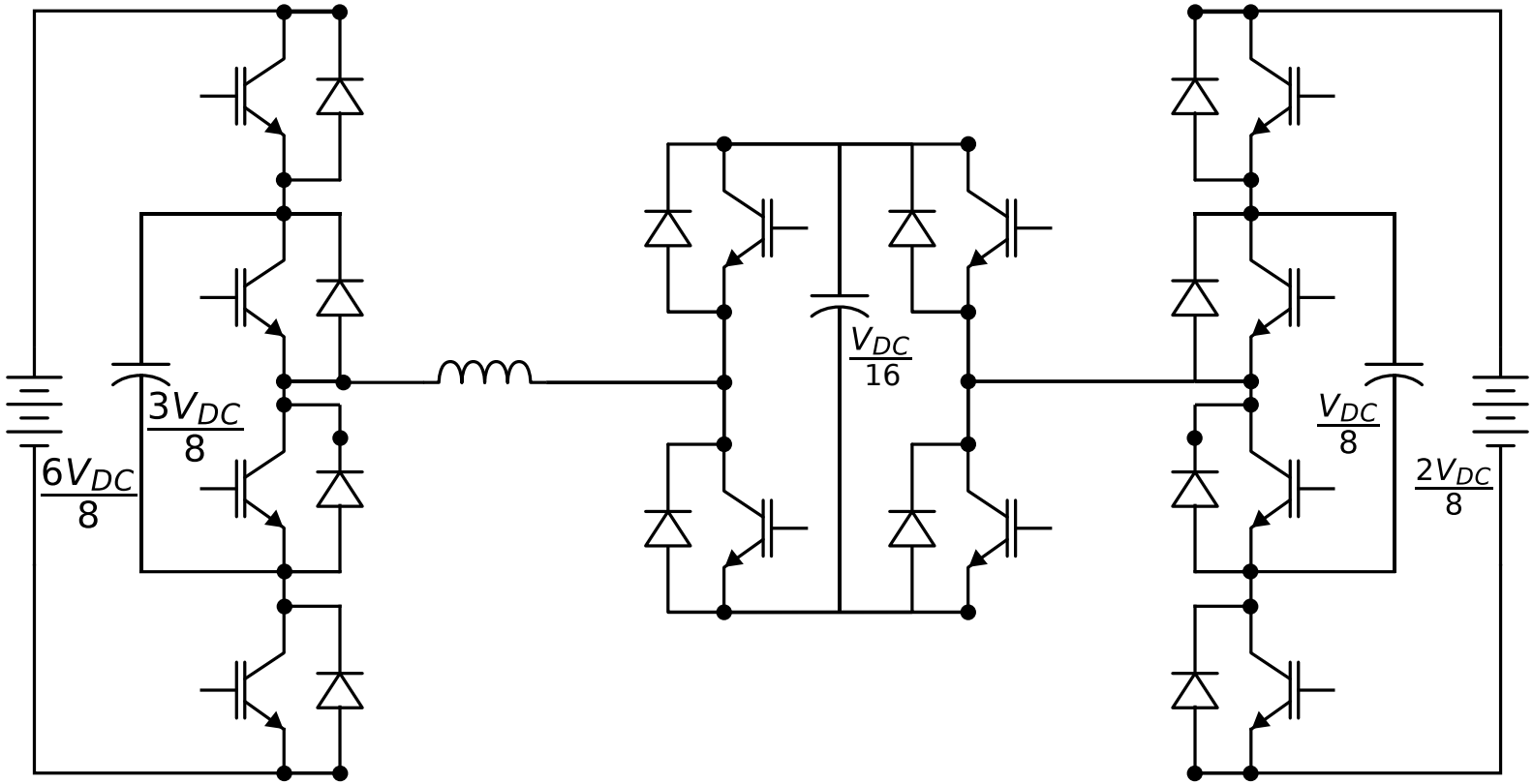
Figure: Experimental results for 45Hz operation (a) Voltage and current waveforms. X-Axis: 5ms/div. (1) A-phase voltage (Y -axis: 200 V/div). (2) Inverter-1 pole voltage V_{AO} (Y -axis: 200V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y -axis: 50V/div). (4) A Phase current (Y -axis: 1A/div) (b) Capacitor voltage waveforms. X-Axis: 5ms/div. (1) Ripple in flying capacitor C1A, (AC coupled) (Y -axis: 5 V/div). (2) Ripple in flying capacitor C2A, (AC coupled) (Y -axis: 200mV/div). (3) A-phase voltage (Y -axis: 100 V/div). (4) A Phase current (Y -axis: 1A/div).

Seventeen Level Inverter Topology for Open End Induction Motor Drive

Circuit Topology (Per-phase)



Circuit Topology (Per-phase)



Effective Pole Voltage

- Inverter-1 is a three level inverter (0, $3V_{DC}/8$, $6V_{DC}/8$)
- Inverter-2 is a seven level inverter (-$0.5V_{DC}/8$, 0, $0.5V_{DC}/8$, $1V_{DC}/8$, ..., $2.5V_{DC}/8$)
- Total of 3x7=21 combinations

Level	$\mathbf{V_{AA'}}$	$\mathbf{V_{AO}}$	$\mathbf{V_{A'O'}}$
0	$-2.5V_{DC}/8$	0	$2.5V_{DC}/8$
1	$-2V_{DC}/8$	0	$2V_{DC}/8$
2	$-1.5V_{DC}/8$	0	$1.5V_{DC}/8$
3	$-1V_{DC}/8$	0	$1V_{DC}/8$
4	$-0.5V_{DC}/8$	0	$0.5V_{DC}/8$
5	0	0	0
6	$0.5V_{DC}/8$	0	$-0.5V_{DC}/8$
6	$0.5V_{DC}/8$	$3V_{DC}/8$	$2.5V_{DC}/8$
7	$V_{DC}/8$	$3V_{DC}/8$	$2V_{DC}/8$
8	$1.5V_{DC}/8$	$3V_{DC}/8$	$1.5V_{DC}/8$
9	$2V_{DC}/8$	$3V_{DC}/8$	$1V_{DC}/8$
10	$2.5V_{DC}/8$	$3V_{DC}/8$	$0.5V_{DC}/8$
11	3	$3V_{DC}/8$	0
12	$3.5V_{DC}/8$	$3V_{DC}/8$	$-0.5V_{DC}/8$
12	$3.5V_{DC}/8$	$6V_{DC}/8$	$2.5V_{DC}/8$

Level	$\mathbf{V_{AA'}}$	$\mathbf{V_{AO}}$	$\mathbf{V_{A'O'}}$
12	$3.5V_{DC}/8$	$6V_{DC}/8$	$2.5V_{DC}/8$
13	$4V_{DC}/8$	$6V_{DC}/8$	$2V_{DC}/8$
14	$4.5V_{DC}/8$	$6V_{DC}/8$	$1.5V_{DC}/8$
15	$5V_{DC}/8$	$6V_{DC}/8$	$1V_{DC}/8$
16	$5.5V_{DC}/8$	$6V_{DC}/8$	$0.5V_{DC}/8$
17	6	$6V_{DC}/8$	0
18	$6.5V_{DC}/8$	$6V_{DC}/8$	$-0.5V_{DC}/8$

Pole Voltage Redundancy

- Inverter-2 needs to be seven-level.
- Extreme levels (0 and 18) not used
- CHB Inverter acts as a 'filter' - cannot deliver power

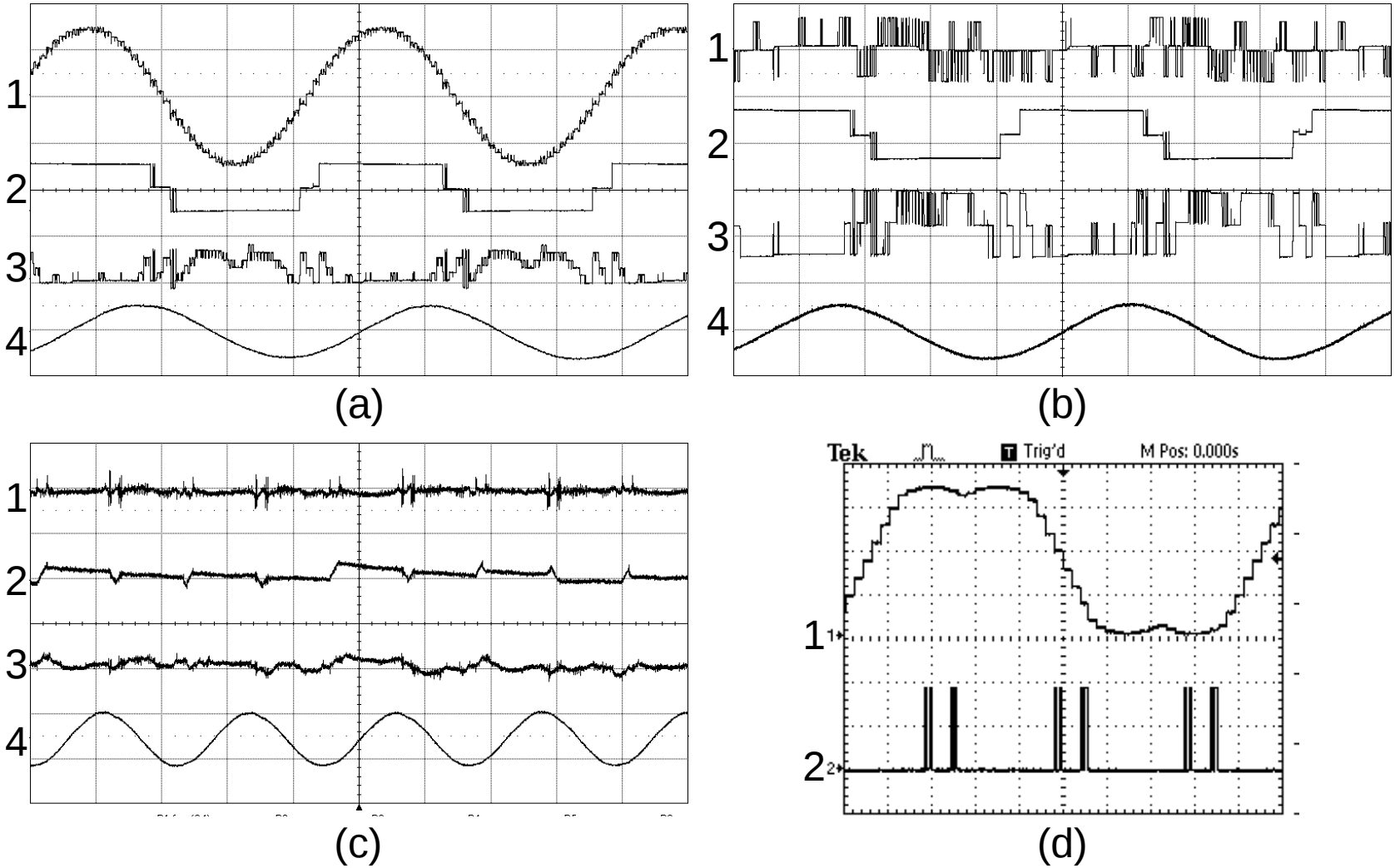


Figure: 45Hz Operation: (a) VAO, VA'O', VAA', IA (b) VA'A",VAO,VA"O', IA (c) VC3A, VC1A VC1A, IA (d) VA_{ref}, Spl. Loc.

Key Contributions

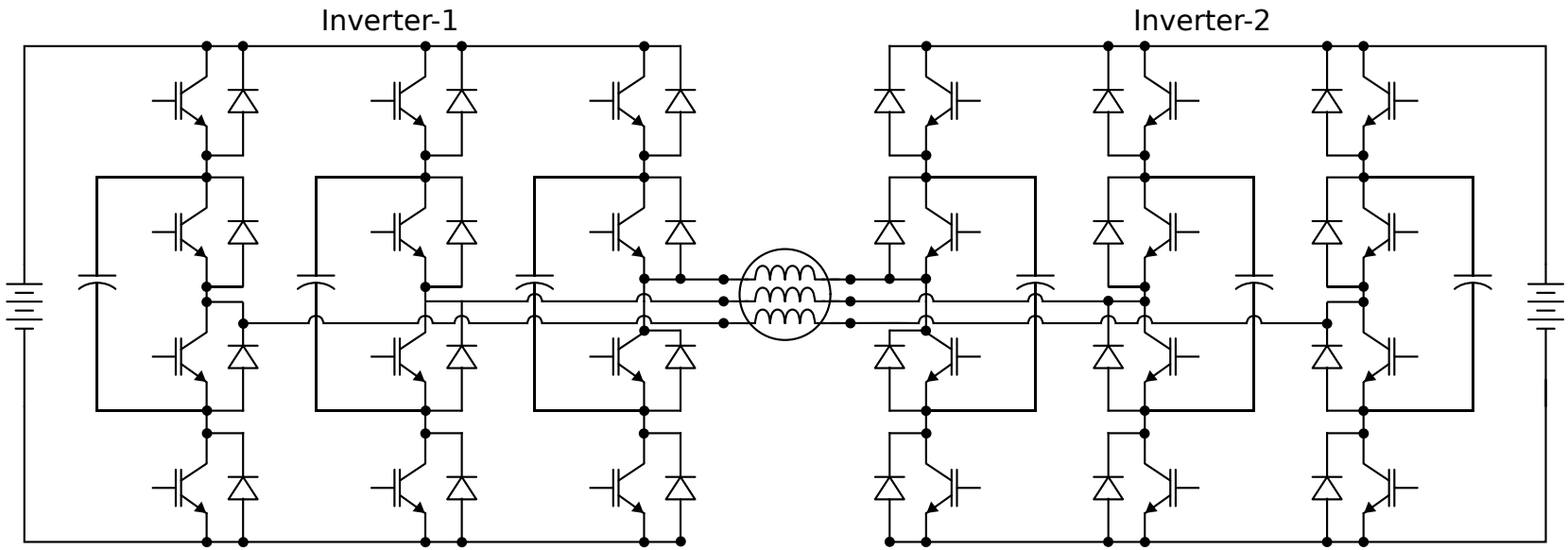
- Two novel inverter topologies proposed with low switch counts:
  - Nine-level inverter with only eight switches and two capacitors per phase
  - Seventeen-level inverter with only twelve switches and three capacitors per phase
- Switching state selection scheme for both with:
  - Capacitor voltage balancing over full modulation range for any load power factor
  - Iteration-less determination of switching state
  - Elimination of DC bus overcharging

THANK YOU

Appendix

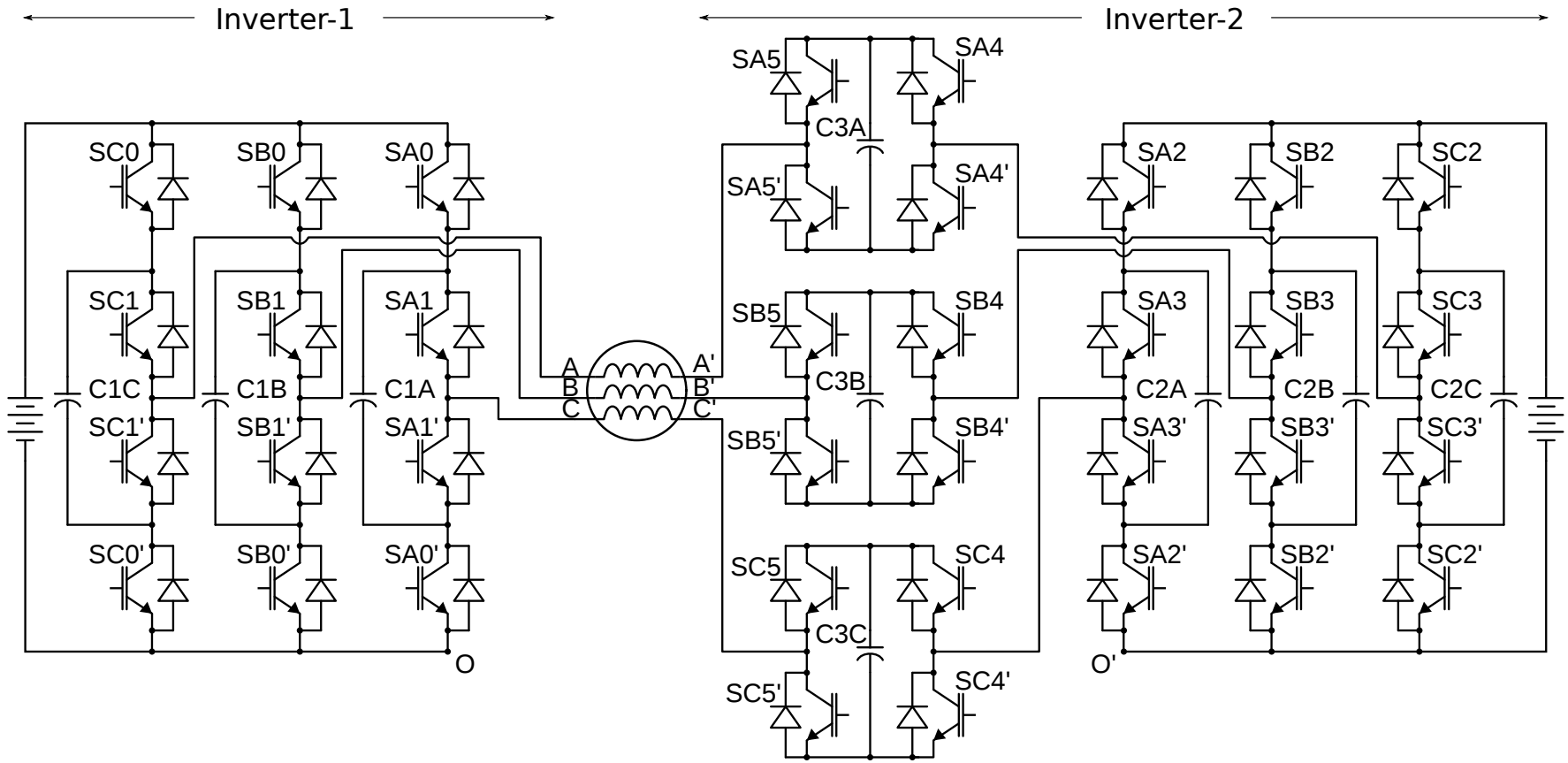
Circuit topology

Proposed Topology for Nine-Level Inverter

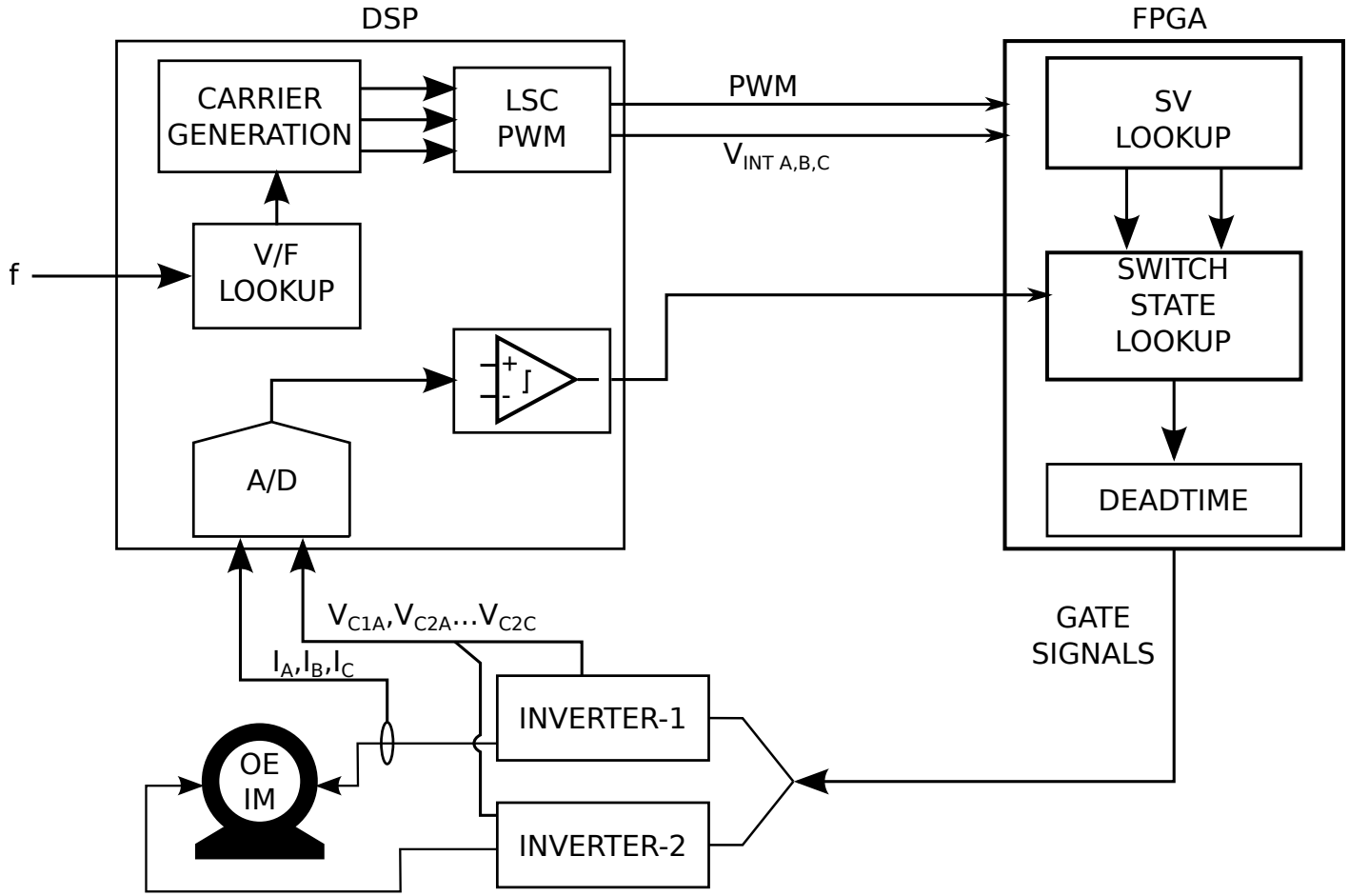


Circuit Topology

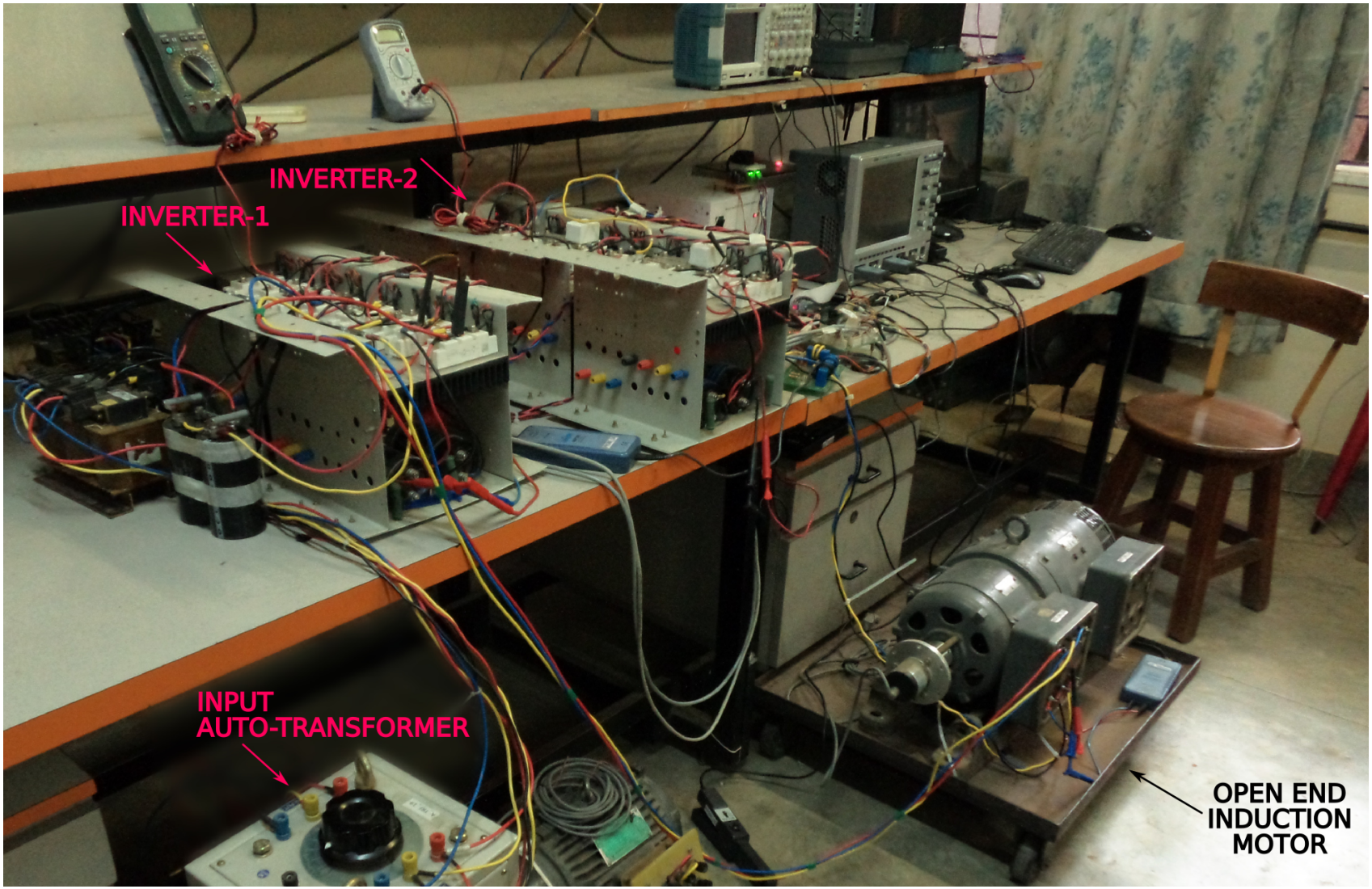
Proposed Topology for Seventeen-Level Inverter



Experimental setup



Setup for experiments



Setup for experiments