Investigations on Stacked Multilevel Inverter Topologies for Induction Motor Drives

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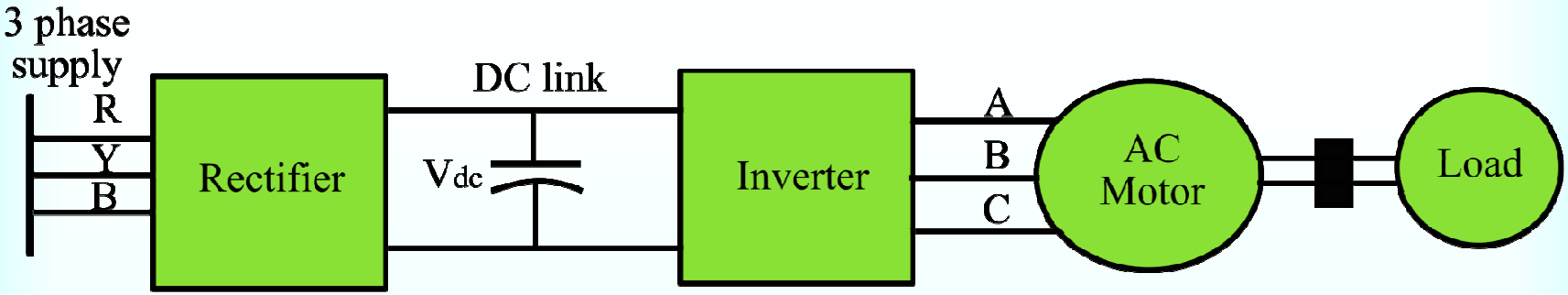
Overview of presentation

- Adjustable speed AC drive systems
- Multilevel inverters and their features
- Motivation for stacked multilevel inverters
- Nine level stacked inverter for 3-phase IM drives
- Conclusion and future scope

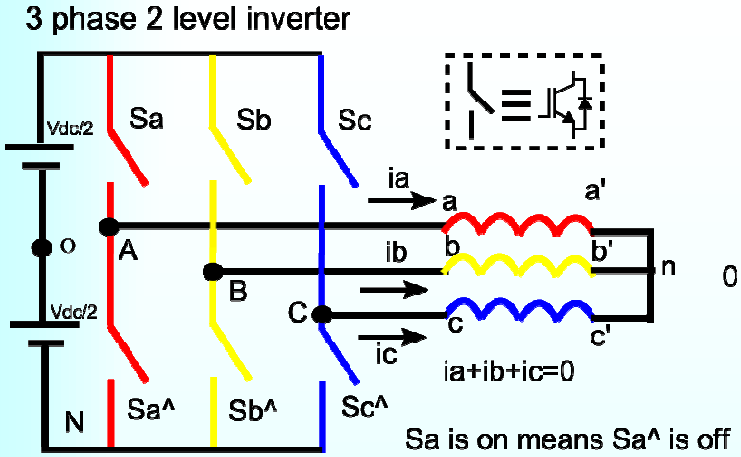
Adjustable speed AC drive system

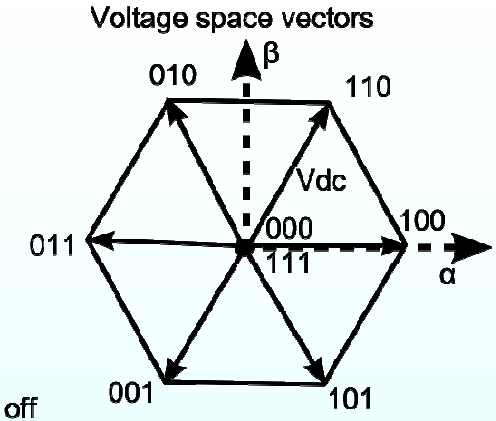


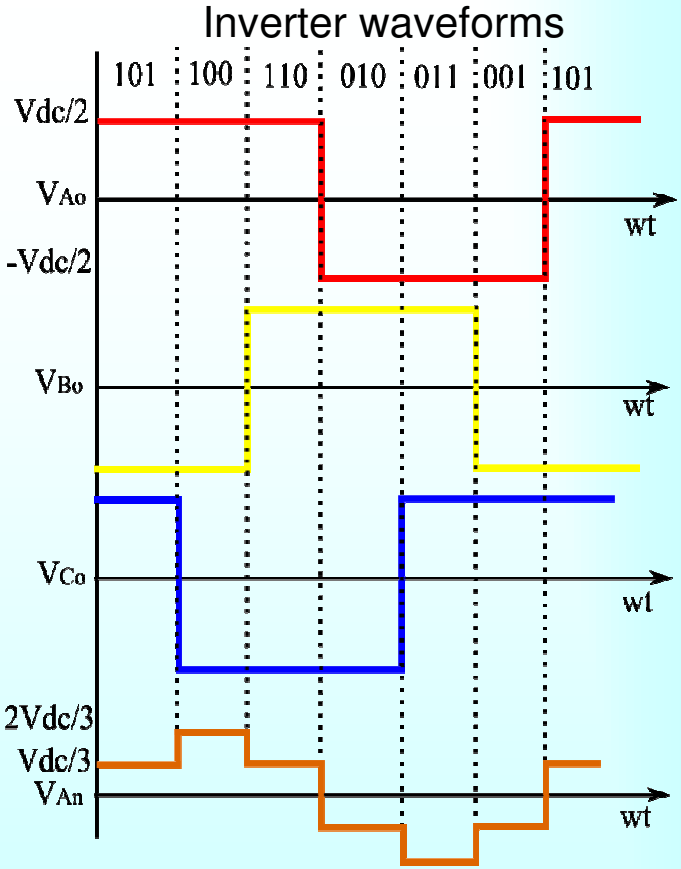
Important modules of an adjustable speed AC drive system are,

- Rectifier
- Three phase Inverter
- AC motor

3 phase conventional two level Inverter







- 8 (2^3) switching states possible
- Only 2 voltage levels in the pole voltage waveforms Hence called as two level inverter

- V_{Ao} is defined as inverter pole voltage.
- V_{An} is defined as motor phase voltage.

Multilevel inverters and their features

Multilevel inverters have more number of levels in the pole voltages and therefore have the following additional features

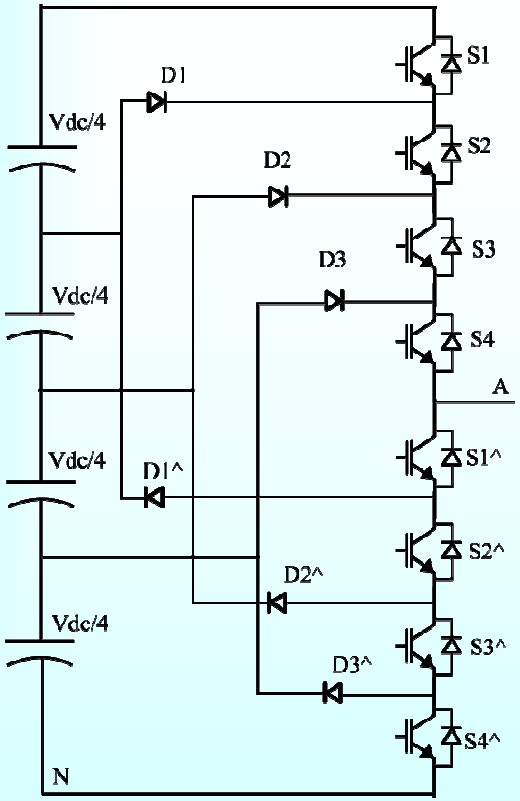
- Improved voltage and current THD
- Reduced switching frequency
- Reduced EMI issues
- Reduced filtering requirements

Commonly used multilevel inverter topologies are

- Diode clamped inverter
- Flying capacitor inverter (FC)
- Cascaded H-bridge inverter (CHB)
- Hybrid multilevel inverter

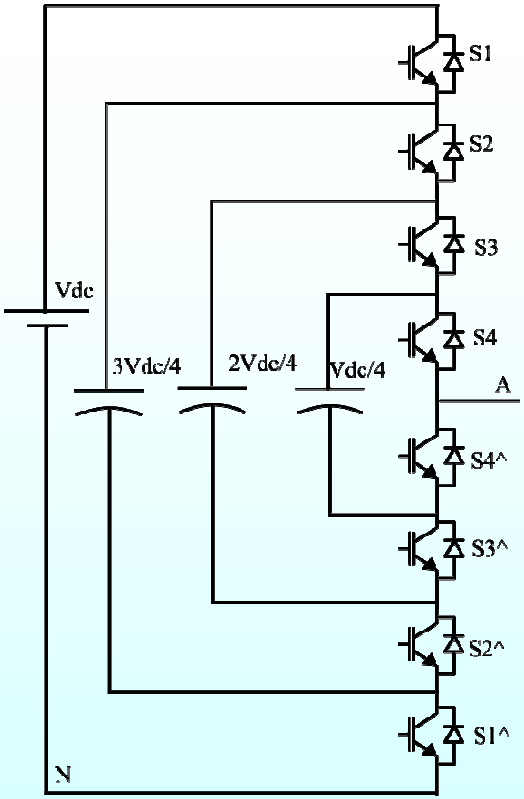
Multilevel inverter topologies

5 level diode clamped inverter



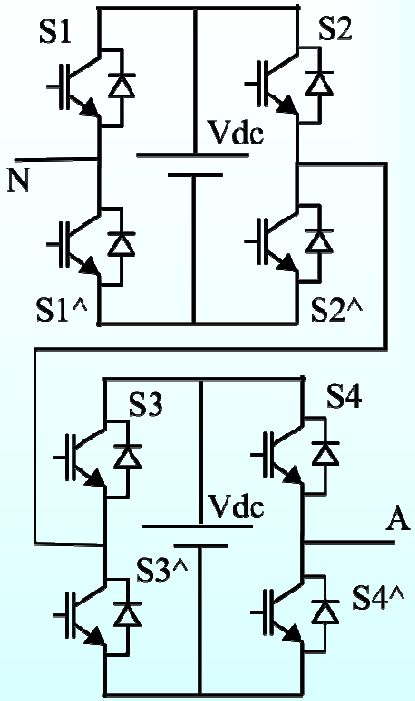
- Requires clamping diodes
- DC link capacitor voltage balancing is difficult

5 level flying capacitor inverter



- As the number of voltage levels increases capacitor voltage balancing is difficult

5 level cascaded H-bridge inverter

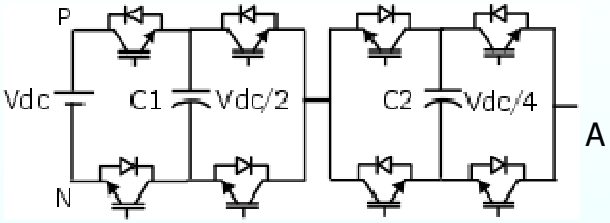


- Modular structure
- Requires multiple DC supply for operation

Multilevel inverters……continued

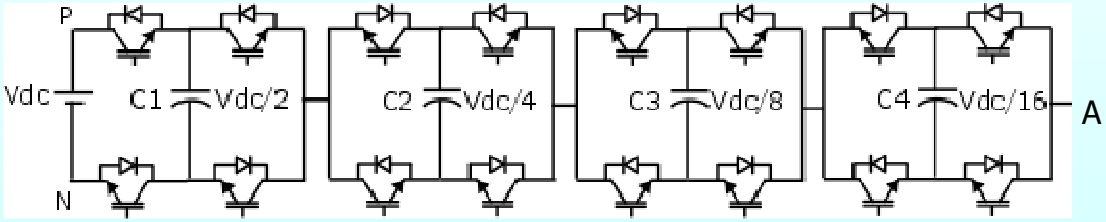
- Hybrid multilevel inverters by combining FC and CHBs

  - 5-level Inverter [1] :



Generates pole voltages: 0, Vdc/4, 2Vdc/4, 3Vdc/4, Vdc (V_{AN})

  - 17-level Inverter [2]:



Generates pole voltages: 0, Vdc/16, 2Vdc/16, 3Vdc/16,…. Vdc (V_{AN})

[1] P. Roshan kumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. Leon, and L. Franquelo, "A five-level inverter topology with single-dc supply by cascading a flying capacitor inverter and an h-bridge," IEEE Trans.Power Electron., vol. 27, no. 8, pp. 3505–3512, Aug 2012.

[2] P.Roshan Kumar, S. Kaarthik, K. Gopakumar, J. Leon, and L. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor h-bridges," IEEE Trans. Power Electron., vol. 30, no. 7, pp. 3471–3478, July 2015.

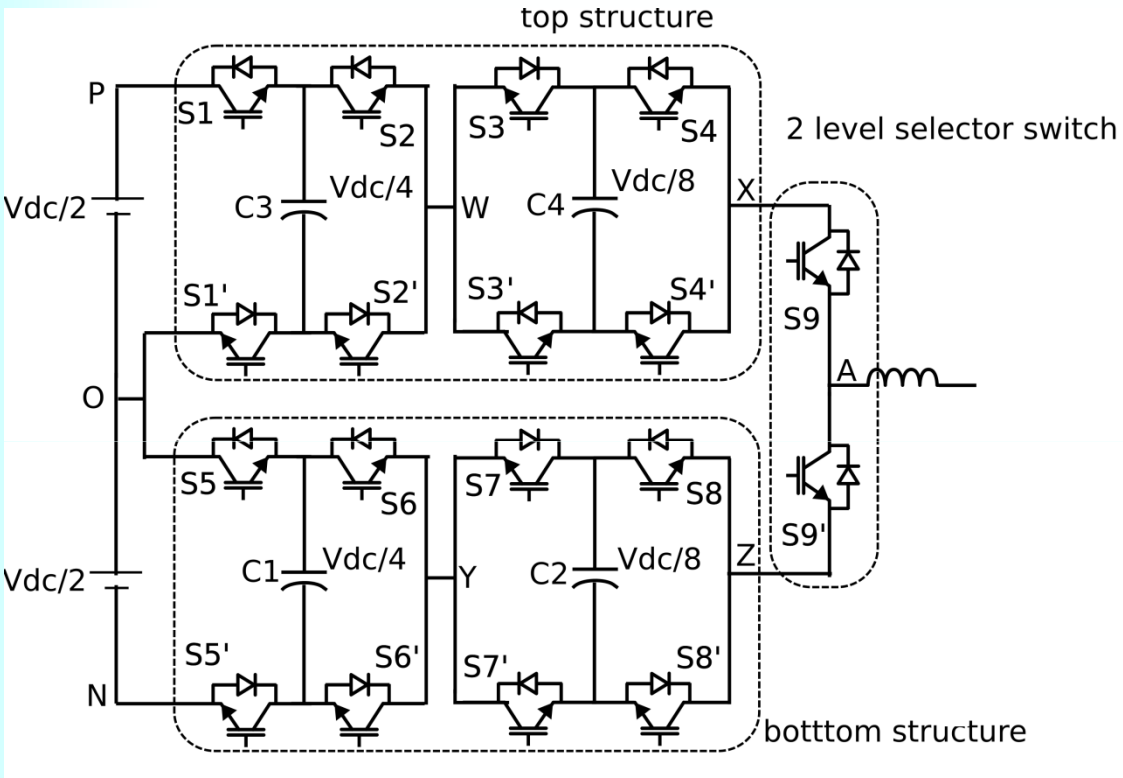
Motivation for stacked inverters

- Basic Inverter topologies when extended to higher levels face difficulties in capacitor balancing like in diode clamped and flying capacitor inverters
- Also their device count drastically increases on increasing the number of levels
- Cascaded H-bridge inverters needs multiple isolated DC sources which limits its applications
- Hybrid inverters formed by combination of FC and CHB cannot be scaled for obtaining higher number of levels since the capacitor voltages match with the switch voltage drops

A new method for generating higher number of levels in the voltage waveform - Stacked Multilevel Inverters

Generation of Higher number of Voltage Levels by Stacking Inverters of Lower Multilevel Structures with Low Voltage Devices for Drives

Nine level stacked inverter



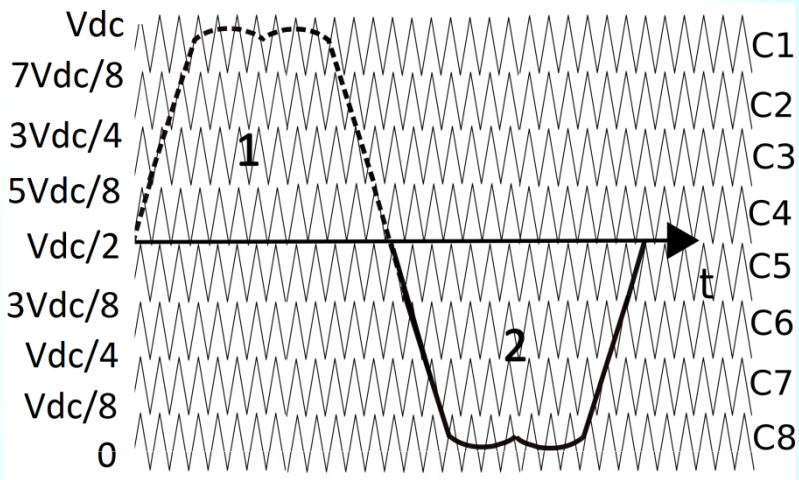
Power circuit schematic for the stacked 9-level inverter by stacking two 5-level inverters for phase 'A'

- Bottom structure generates pole voltages (V_{ZN}): 0, Vdc/8, Vdc/4, 3Vdc/8, Vdc/2 with respect to 'N'
- Top structure generates same pole voltages with respect to 'O' (V_{XO})
- With respect to 'N', top structure generates Vdc/2, 5Vdc/8, 3Vdc/4, 7Vdc/8, Vdc (V_{XN})
- Thus stacked inverter generates the nine pole voltages (V_{AN})
- 2-level selector switch connects the respective outputs to the machine terminals

Note: S1-S1', S2-S2'…..S9-S9' are complimentary switches

Stacked inverter……continued

- Top structure modulates the section-1and bottom structure modulates the section-2 to generate the respective pole voltages
- So the selector switches need to switch only at fundamental frequency
- In each carrier region, the carrier and modulating signal are compared and the pole voltage switch between the 2 levels



Carrier based PWM

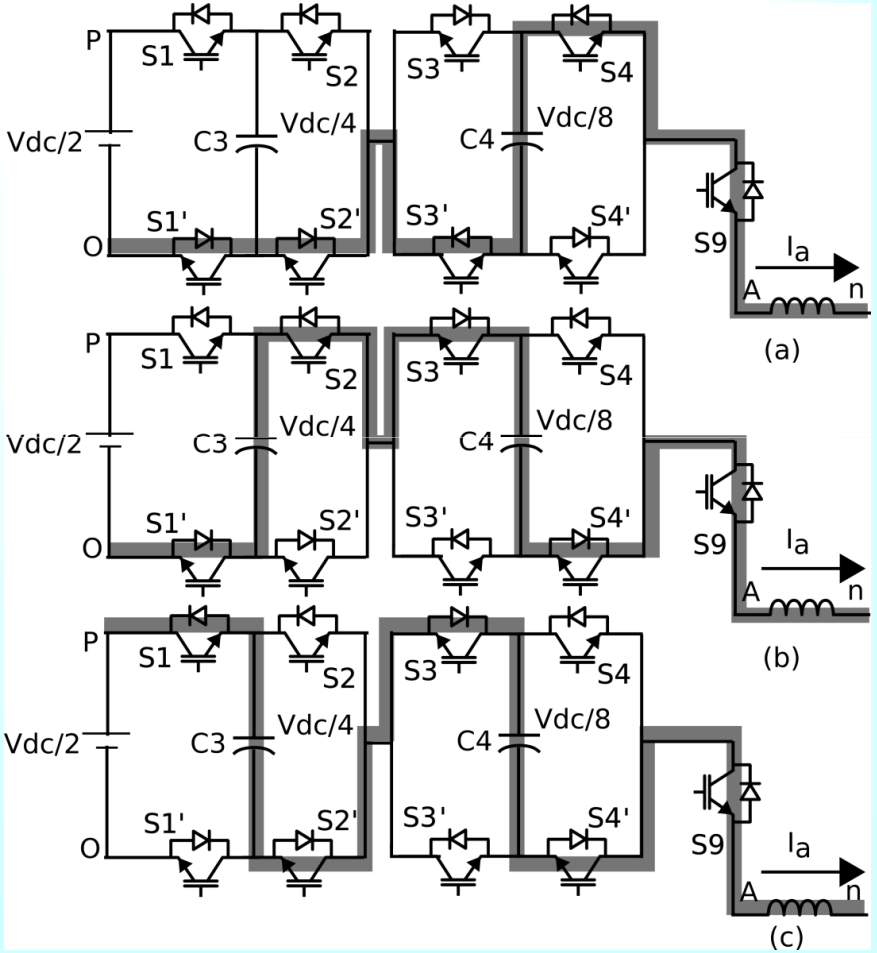
- Above pole voltages will be generated only if the capacitor voltages are maintained at their respective values
- This is achieved using the switching state redundancies available with each of the pole voltages

Stacked inverter - capacitor voltage control example

The 3 figures shows the multiple ways to achieve a pole voltage of 5Vdc/8

Fig	Switching state	C3	C4
a	0001	Unaffected	Discharging
b	0110	Discharging	Charging
c	1010	Charging	Charging

- The table is for positive direction of current
- A tolerance band is defined for each of the capacitor voltage references
- Appropriate switching state is selected to maintain the voltages
- Switching state redundancies exist for all the pole voltages



Note: '1' indicates top switch is ON. '0' indicates bottom switch is ON

Capacitor voltage control…….continued

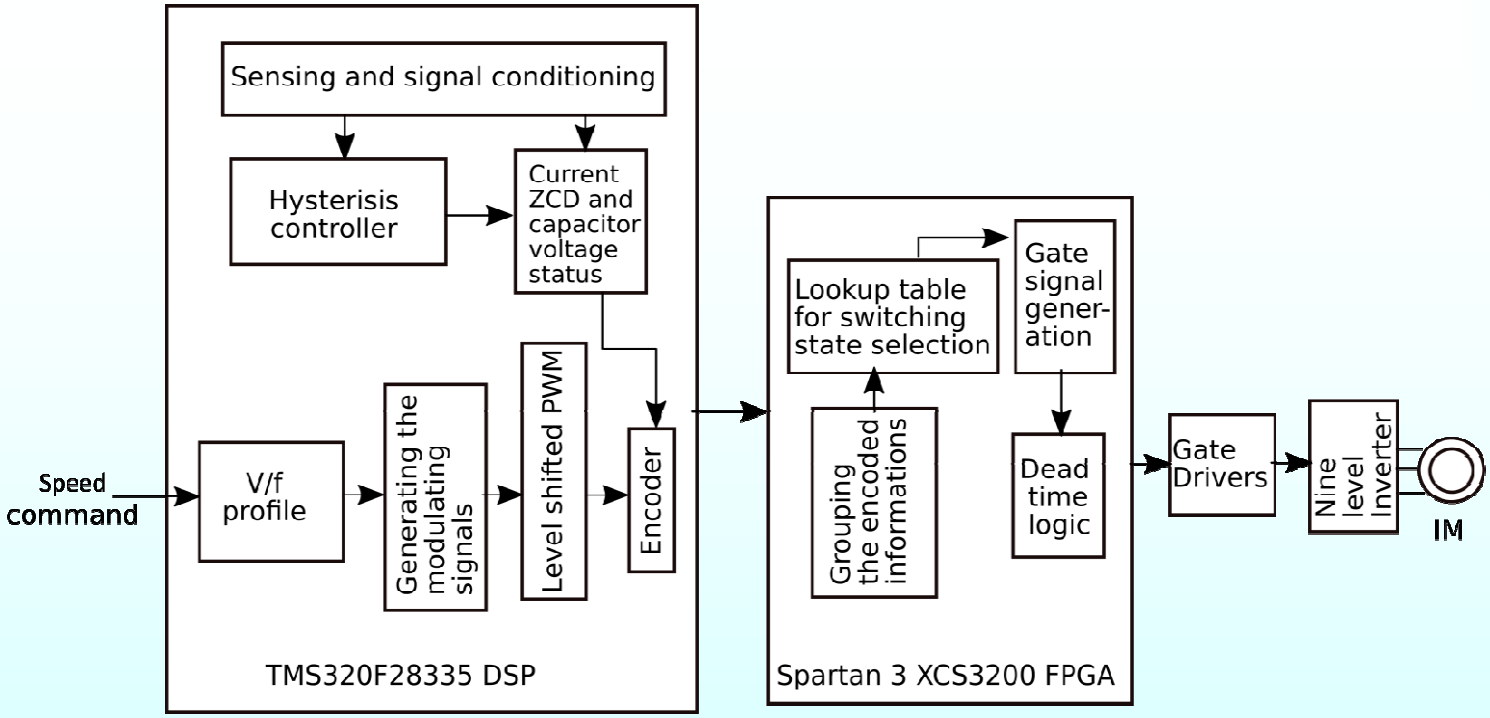
- So a switching state is finally decided by the pole voltage, capacitor voltage status (H_{ax}, x=1,2,3,4) and the current direction as shown in the table

Ia	Ha1/Ha3	Ha2/Ha4	Switching State Selected (S1,S2,S3…S9)		
			Vdc/8	Vdc/4	3Vdc/8
+	0	0	000010100	000010110	000011100
+	0	1	000000010	000010110	000010010
+	1	0	000001100	000001110	000011100
+	1	1	000000010	000001110	000001010
-	0	0	000000010	000001110	000001010
-	0	1	000001100	000001110	000011100
-	1	0	000000010	000010110	000010010
-	1	1	000000010	000010110	000011100
"+" indicates current flowing out from pole "A" . Switch state "1" indicates switch is ON. H_{ax}=1 implies capacitor needs discharging to maintain voltages with in tolerance band					

- All the capacitor voltages and current directions are sensed in DSP and send to FPGA in every switching cycle along with pole voltage and PWM timing

- Above table is stored in FPGA which selects the correct switching state based on the inputs from DSP

Implementation block diagram



- Switching frequency = 2kHz
- 3-phase, 415V,7.5kW, 50Hz IM is used
- All the capacitors are 2200uF

Capacitor sizing

- The capacitor sizing is done by using the relation,

$$C = \frac{I_p}{f_s * \Delta V}$$

***where*,**

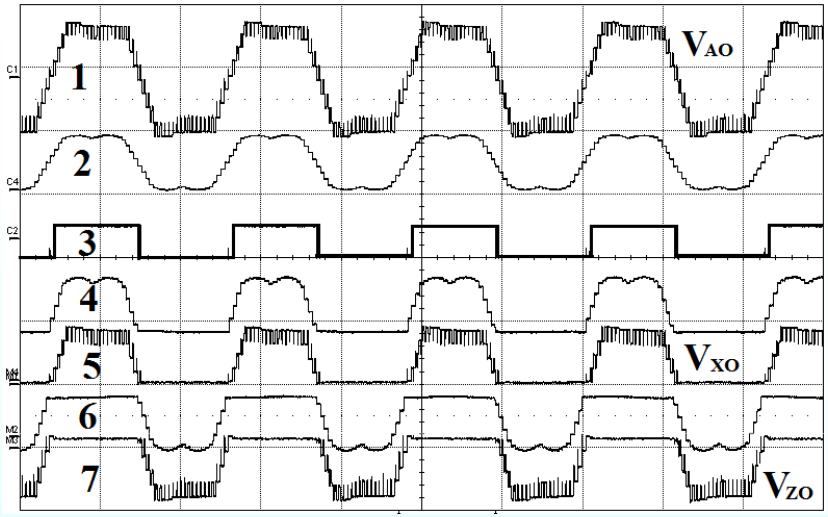
I_p = **peak capacitor current (10A)**

f_s = **minimum sampling frequency (1800Hz)**

ΔV = **peak to peak capacitor voltage ripple (2.5V)**

- So for conducting the experiment, the capacitance value is selected as 2200μF for all the three phases

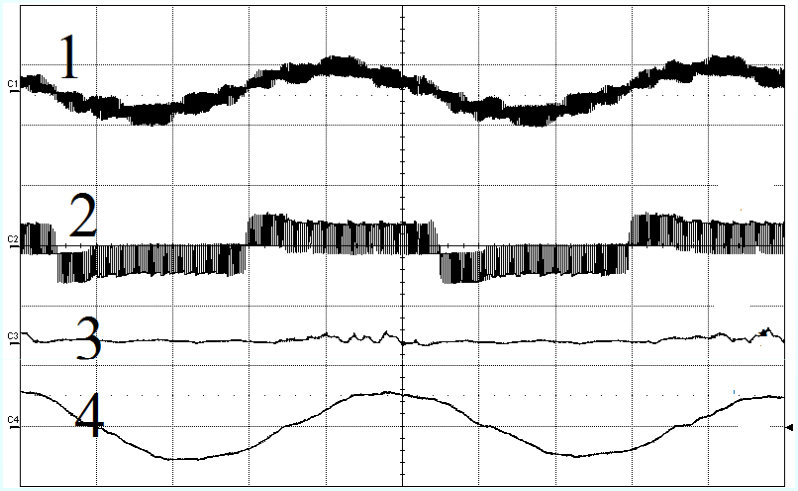
Experimental results



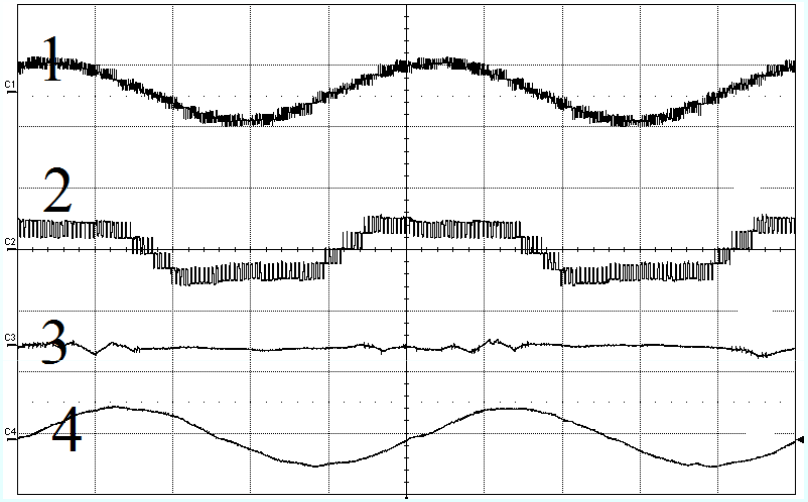
(a) Modulating signal and generated pole voltages
x-axis: 10ms/div

1) Inverter pole voltage (V_{AO}) : 100V/div
2) Modulating signal
3) Gate signal to selector switch
4) Positive half of modulating signal
5) Top structure pole voltage (V_{XO}): 20V/div
6) Negative half of modulating signal
7) Bottom structure pole voltage (V_{ZO}): 100V/div

Experimental results at steady state



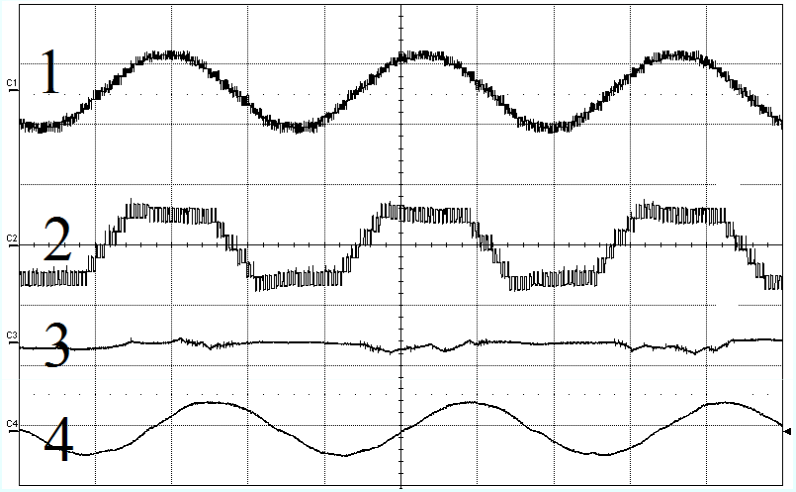
(b) 10Hz , x-axis: 20ms/div



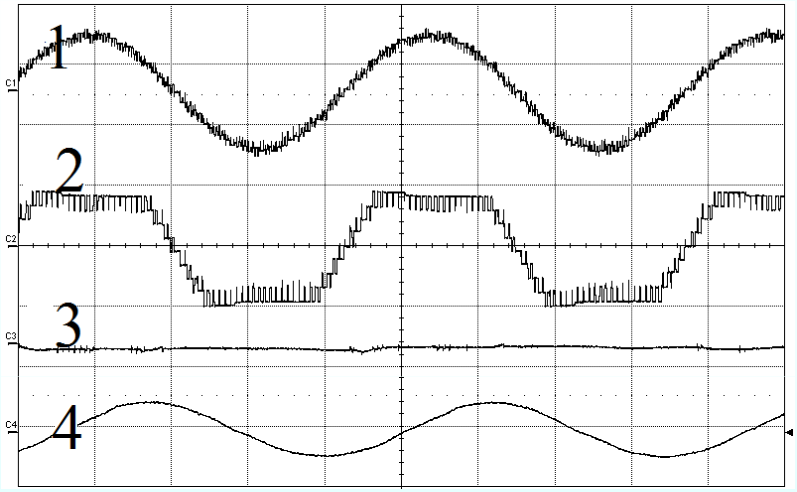
(c) 20Hz , x-axis: 10ms/div

1) Motor phase voltage (V_{An}) : 100V/div
2) Inverter pole voltage (V_{AO}): 100V/div
3) Capacitor voltage ripple (V_{c3}): 5V/div
4) Phase current (I_a): 2A/div.

Steady state results ……continued



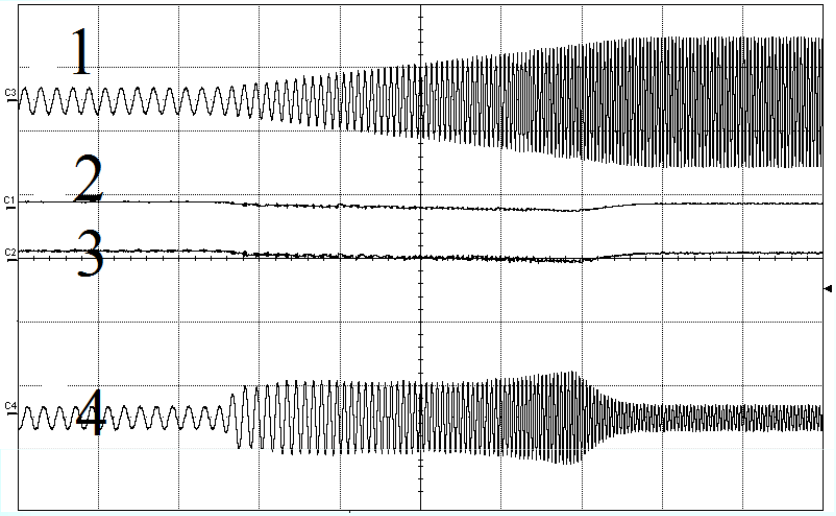
(d) 30Hz , x-axis: 10ms/div



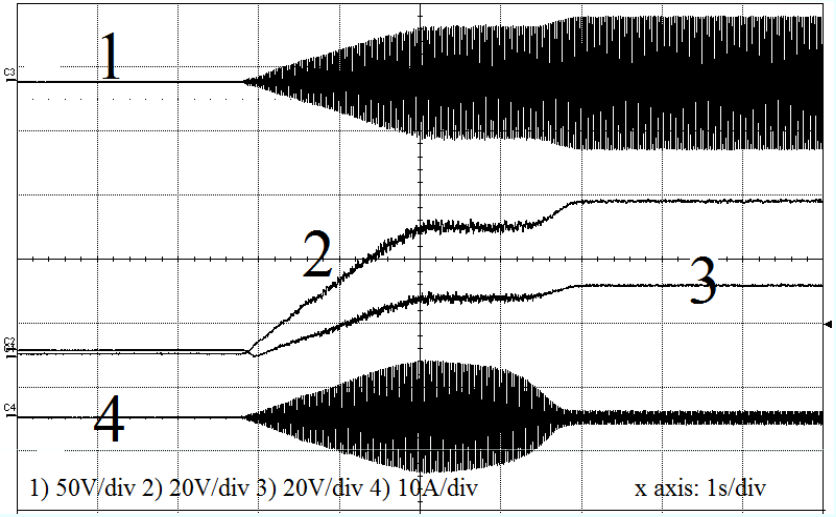
(e) 45Hz , x-axis: 5ms/div

1) Motor phase voltage (V_{An}) : 100V/div
2) Inverter pole voltage V_{AO}): 100V/div
3) Capacitor voltage ripple (V_{c3}): 5V/div
4) Phase current (I_a): 2A/div.

Transient results



(f) Motor acceleration, x-axis: 500ms/div

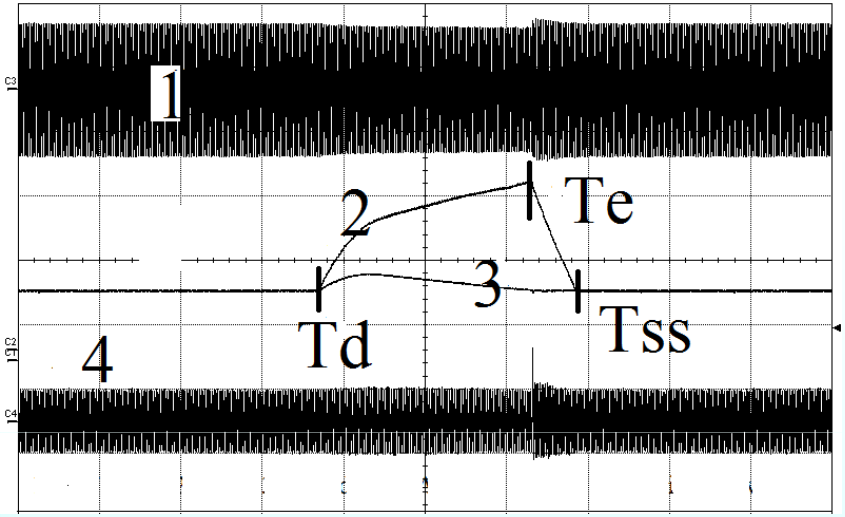


(g) Motor starting, x-axis: 1s/div

1) Motor phase voltage (V_{An}) : 50V/div
2) Capacitor voltage ripple (V_{c4}): 5V/div
3) Capacitor voltage ripple (V_{c3}): 5V/div
4) Phase current (I_a): 5A/div.

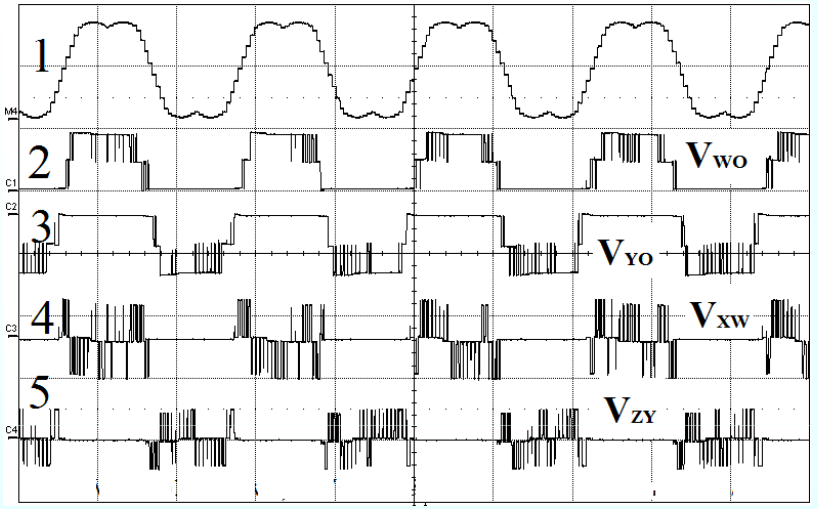
1) Motor phase voltage (V_{An}) : 50V/div
2) Capacitor voltage (V_{c4}): 20V/div
3) Capacitor voltage (V_{c3}): 20V/div
4) Phase current (I_a): 10A/div.

Experimental results…….continued



(h) Capacitor balancing test, x-axis: 10ms/div

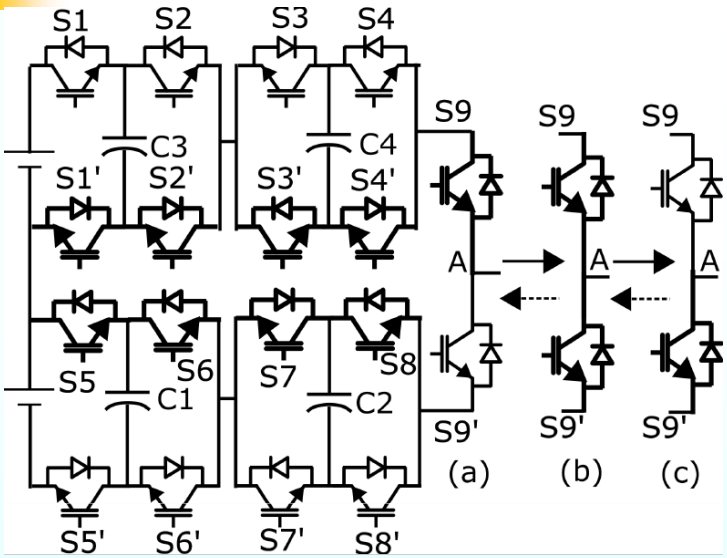
1) Motor phase voltage (V_{An}) : 50V/div
2) Capacitor voltage (V_{c4}): 20V/div
3) Capacitor voltage (V_{c3}): 50V/div
4) Phase current (I_a): 2A/div.



(i) FC and H-bridge switching, x-axis: 5ms/div

1) Modulating signal
2) Top FC pole voltage: 100V/div
3) Bottom FC pole voltage: 100V/div
4) Top H-bridge switching : 20V/div
5) Bottom H-bridge switching: 50V/div

Soft cycle commutation for selector switches

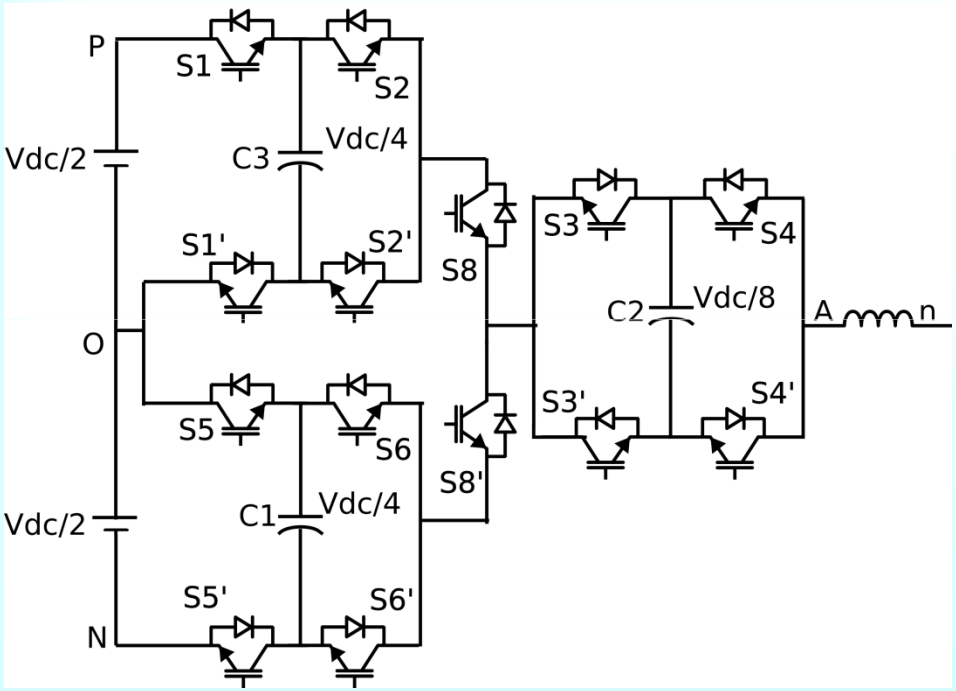


In figure, darkened switches are ON

- When the bottom structure is operating, switches, S1', S2', S3', S4' are kept ON
- When the top structure is operating, switches S5, S6, S7, S8 are kept ON
- It is done to reduce the voltage rating of selector switches to Vdc/2

- When transiting from positive half to negative half cycle, if S9' is turned ON before S9 turns off, then S9 can undergo a zero voltage switching OFF and S9' can undergo a zero voltage switching ON (solid arrow in fig)
- Zero voltage switching can be done during the reverse transition also (dotted arrow)
- It helps to minimize the switching losses in the selector switches

Reduced device count power circuit for stacked inverter [1]



- The H-bridges can be made common by connecting the selector switches in between
- Here the number of switches and capacitors are reduced but now the H-bridges have to switch throughout the cycle
- The FC switches still need to operate only in one half of fundamental cycle
- If the H-bridges fails, inverter can still operate as 5-level inverter in the entire modulation range with rated power

[1] Viju Nair R, Arun Rahul S, Sudarshan Karthick, Abhijit Kshirsagar, K Gopakumar, "*Generation of Higher Number of Voltage Levels by Stacking Inverters of Lower Multilevel Structures with Low Voltage Devices for Drives*", accepted in IEEE Transactions on Power Electronics

Conclusion

- Stacked inverter generates higher number of voltage levels with inherent capacitor balancing capabilities
- All the capacitors can be balanced irrespective of any modulation index and load power factor
- Stacking reduces the DC supply requirement at front end
- The switching loss associated with the selector switches are minimised through soft cycle commutation (switching at fundamental frequency only)
- The FC and H-bridge switches used are of low voltage ratings (Vdc/4, Vdc/8)
- The FC switches need to operate only in one half of fundamental cycle
- The inverter can operate in lower number of voltage levels in case of failure of H-bridge for the rated power in entire modulation range
- This method of stacking can be extended to obtain still higher number of voltage levels and the inverter can be driven directly from low voltage battery cells (EV)