Fully Integrated CMOS Transmitter and Power Amplifier for Software Defined Radios and Cognitive Radios

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Problem Statement

The aim of this thesis is to design a complete transmitter with an integrated power amplifier in CMOS that can serve as an RF front-end for software defined radios. The requirements are:

- Reconfigurability -- to transmit at different carrier frequencies and maintain sufficient output power and efficiency across the entire frequency range.
- Transmit signals with different modulation schemes -- both constant and varying envelope signals.
- Transmit signals with different bandwidths.
- Output power control at all frequencies.

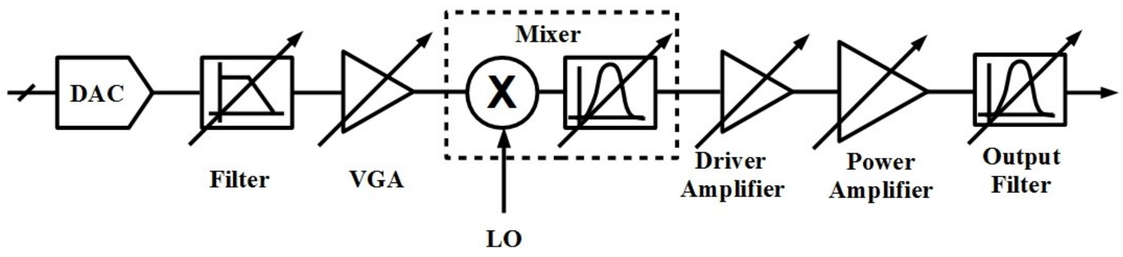


Figure: Modifying a traditional transmitter for SDR.

Proposed Transmitter Architecture

- Digital inputs – I and Q data streams (9-bits wide each)
- RF Input – Continuous wave signal at 2 x f_C
- Clock generation block – generates differential rail-to-rail quadrature clock phases.
- Digital processing block – DPD, 2 levels of filtering.
- Digital mixing
- Tunable RF Power DAC as the output stage.

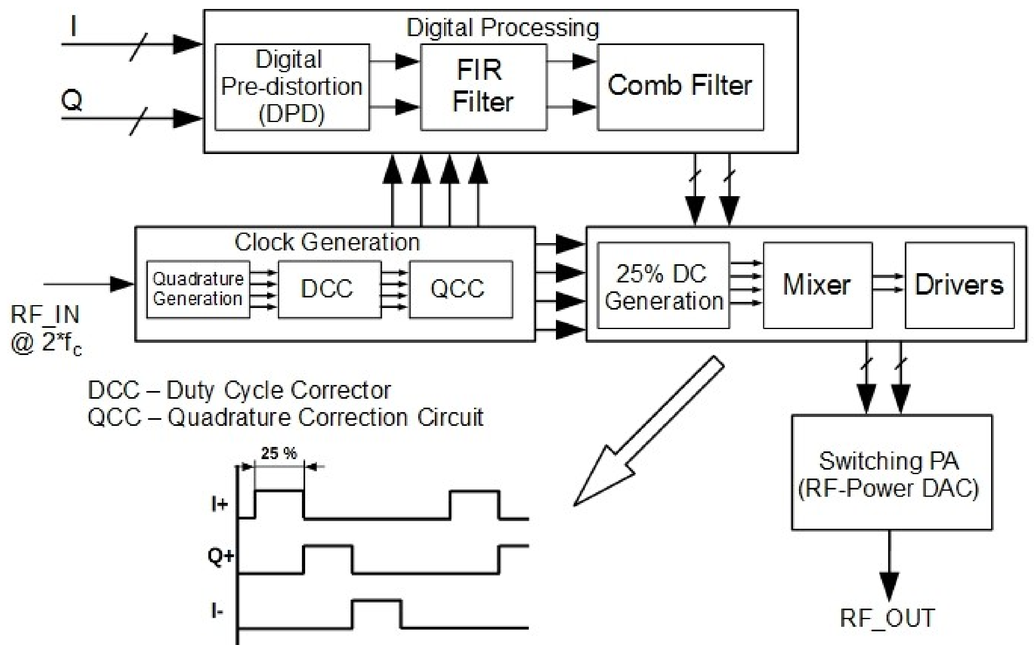


Figure: Proposed transmitter architecture.

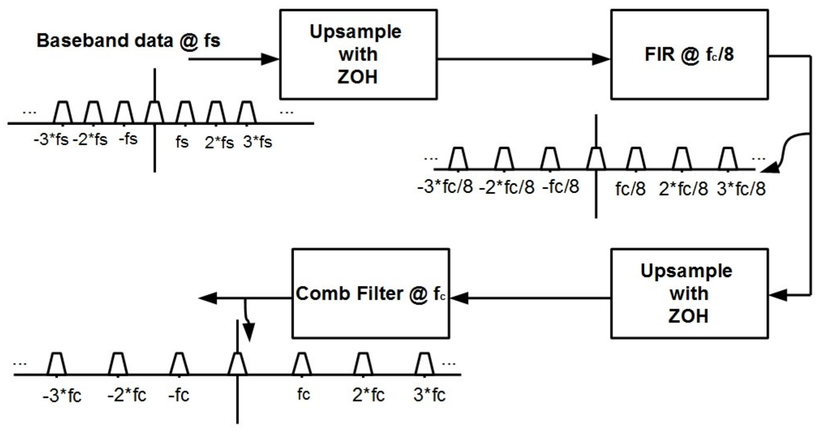


Figure: Digital signal processing for spur suppression.

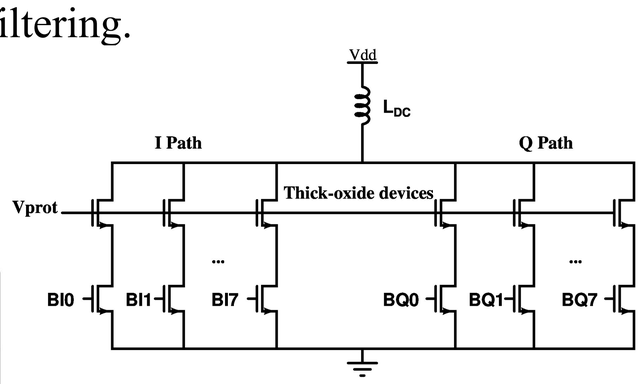


Figure: RF-DAC PA Switches.

Advantages

- Tunability required only at the output stage.
- Reconfiguration of baseband digital filters is much easier to accomplish.
- Scales well with technology.

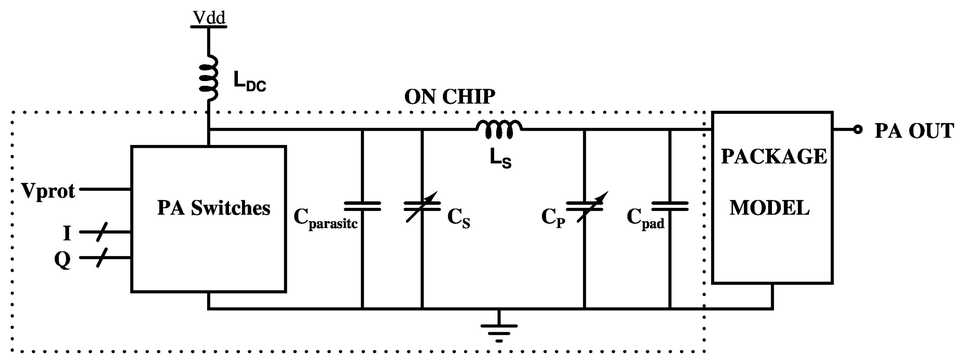
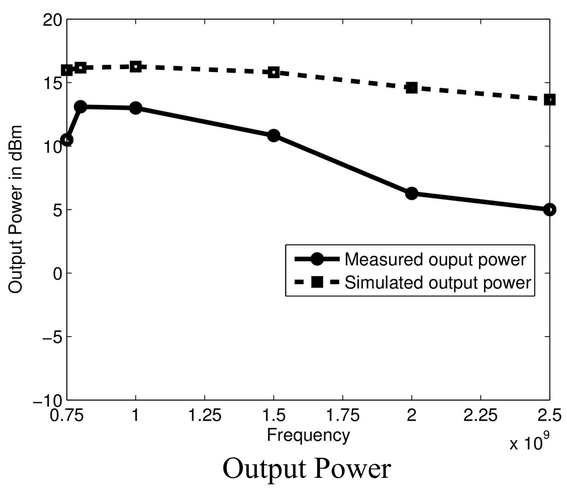
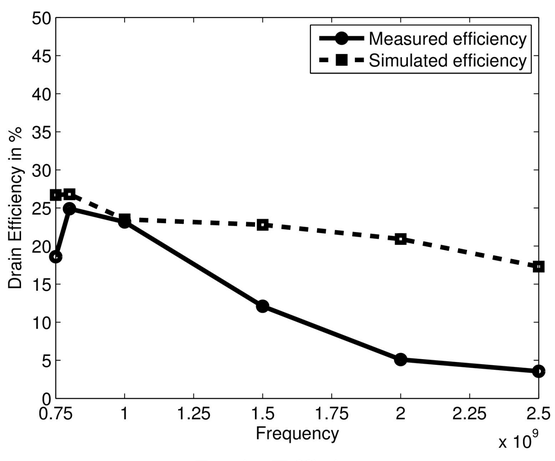


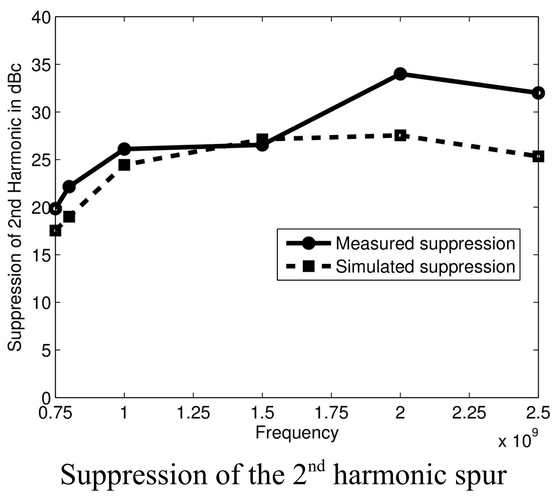
Figure: Reconfigurable Class-E PA Schematic.



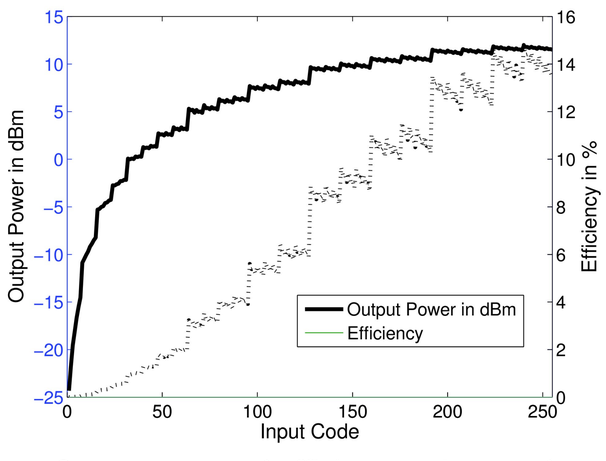
Output Power



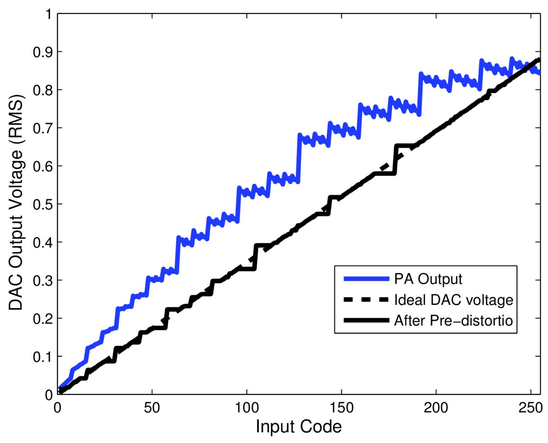
Drain Efficiency



Suppression of the 2nd harmonic spur



Output power and efficiency vs input code



Predistortion to linearize the DAC.

Frequency	800 MHz	1 GHz	2 GHz
EVM (RMS)	3.1%	4%	13.4%
Magnitude Error	1.6%	1.9%	8.3%
Phase Error	2.15 deg	3.5 deg	10.4 deg
Quadrature Error	0.7 deg	1.1 deg	3.6 deg
Gain Imbalance	0.3 dB	0.3 dB	0.14 dB

Measured linearity parameters while transmitting a 16 QAM signal at different carrier frequencies.

Reference	Frequency Range	Architecture	Output Power	Efficiency	Matching Network	Support for Complex / AM Signals	Technology
Shreshtha06	DC-2.4 GHz	Polyphase modulator	8mW	11%	Off-chip RF choke	No	130nm CMOS
Presti09	0.8-2 GHz	Polar TX	23.5-25 dBm	40-47%	Off-chip matching & tuning network	Yes	130nm SOI CMOS
Ingels10	0.75-2.5 GHz	Analog TX	0-4 dBm	NA	On-chip	Yes	40nm CMOS
Hampel12	9 GHz	Analog TX Inductive Degneration	4 dBm	NA	Bondwires as RF Choke	Not reported	65nm CMOS
Moloudi09	900 MHz	Outphasing TX	16-13 dBm	49%	Off-chip combining & matching network	Yes	90nm CMOS
Werquin13	0.9-1.9 GHz	Polar TX	16.7 dBm	12.4%	Off-chip matching network	Yes	65nm CMOS
Analui14	50 MHz-6 GHz	Analog TX	0.2-2.7 dBm	NA	On-chip wideband Trans. Lines	Yes	130nm CMOS
Yin15	0.1-6 GHz	Analog TX 4-band solution	2 dBm	NA	On-Chip	Yes	65nm CMOS
This work	0.75-2.5 GHz	Digital IQ	6.5-13 dBm	27% @ 1 GHz	On-chip RF choke off-chip	Yes	130nm CMOS

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E-Mail: immanuel@ece.iisc.ernet.in

Publications

I. Raja and G. Banerjee, "An inductor-less transmission line based 60 GHz PA in 65-nm CMOS with analog power control," IEEE ICECS, Monte Carlo, 2016, pp. 149-152.
I. Raja, V. Khatri, Z. Zahir and G. Banerjee, "A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS," in IEEE TVLSI Systems, vol. 25, no. 3, pp. 1044-1053, March 2017.
I. Raja, G. Banerjee, M. A. Zeidan and J. A. Abraham, "A 0.1–3.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS," in IEEE TVLSI Systems, vol. 24, no. 5, pp. 1975-1983, May 2016.
J. S. Gaggatur, V. Khatri, I. Raja, M. K. Lenka and G. Banerjee, "Differential multi-phase DLL for reconfigurable radio frequency synthesizer," 2014 IEEE CONECCT, Bangalore, 2014, pp. 1-5.

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Overview

Introduction – Software Defined Radio (SDR)

SDR is "a radio that is substantially defined in software and whose physical layer behaviour can be significantly altered through changes to its software... In other words, the same piece of hardware can be modified to perform different functions at different times, allowing the hardware to be specifically tailored to the application in hand."

J. H. Reed, Software radio: a modern approach to radio engineering. Prentice Hall Professional, 2002.

Benefits of SDR:

- Multifunctionality
- Ease of upgradation
- Obsolescence mitigation
- Global usage.

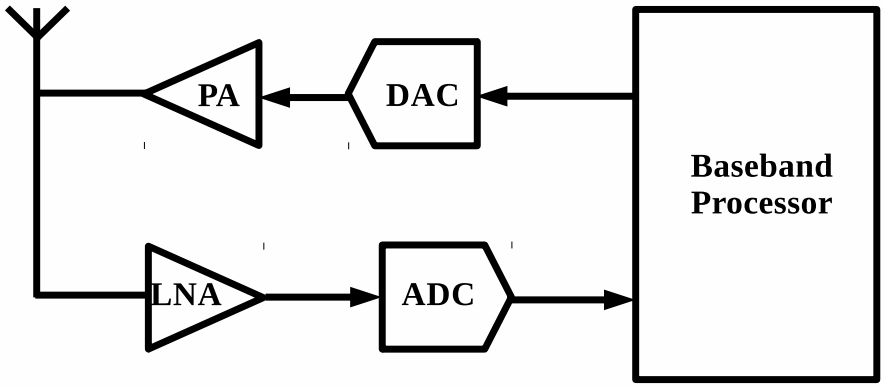

Figure : Block diagram of an ideal SDR transceiver.

Problem Statement

The aim of this thesis is **to design a complete transmitter with an integrated power amplifier in CMOS that can serve as an RF front-end for software defined radios.**

The requirements are:

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- Transmit signals with different modulation schemes – both constant and varying envelope signals.
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Power Amplifier - Classes

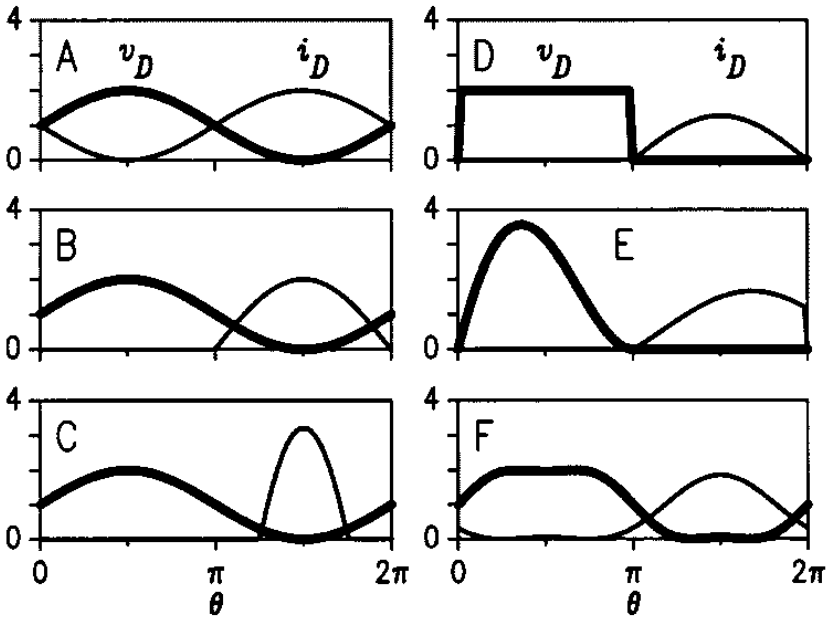


Figure : Voltage and current waveforms for different PA classes.

The Power Amplifier (PA) is at the heart of any transmitter. The architectural design of the transmitter heavily depends on the type of PA used.

- Linear PAs–Classes A, B, AB, C
  Good linearity with poor efficiency. Linearity traded off for efficiency.
- Switching PAs–Classes D, E, F, S
  High Efficiency, but can support only constant envelope signals.

Modifying a Traditional Transmitter for SDR

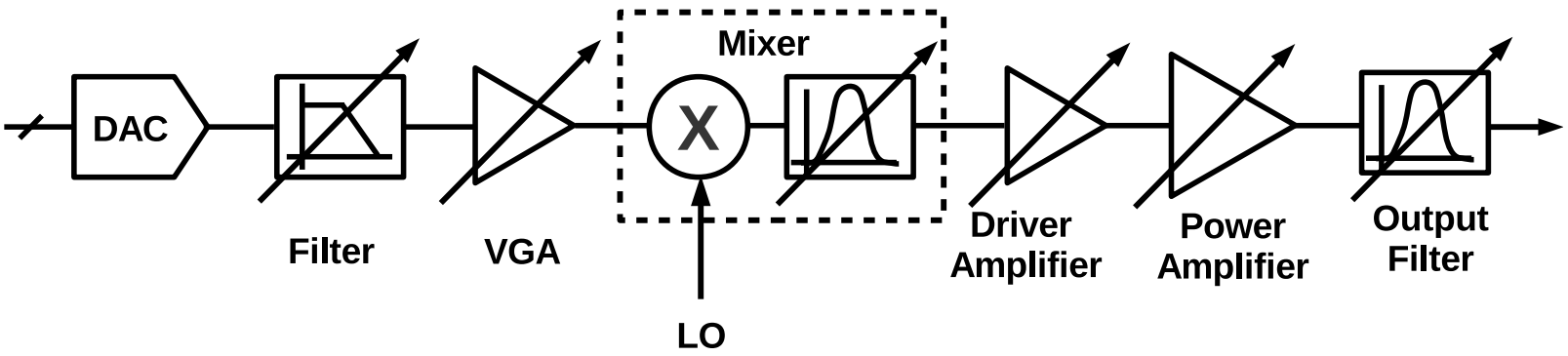
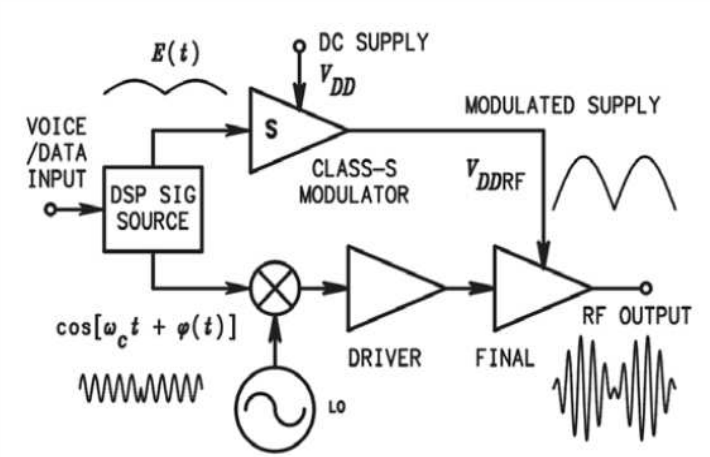


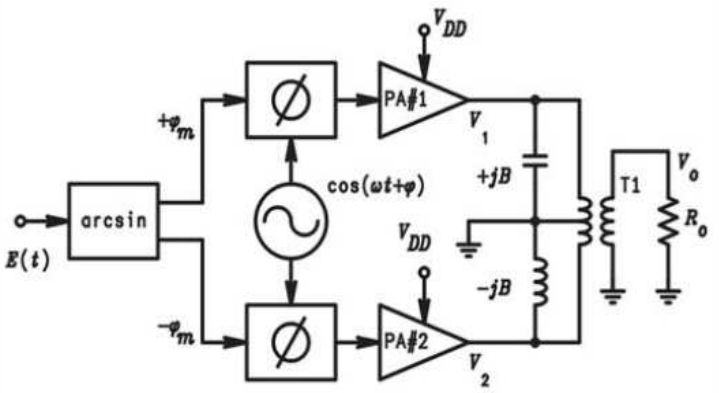
Figure : Traditional transmitter architecture adapted for wideband SDR/CR

- Extremely difficult to implement.
- Tuning one block would affect the other blocks.
- Digital transmitters are better suited for SDR applications.

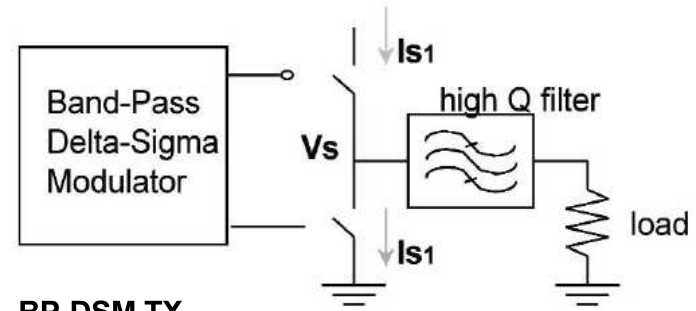
Techniques to use Switching PAs to Transmit Signals with Amplitude Modulation



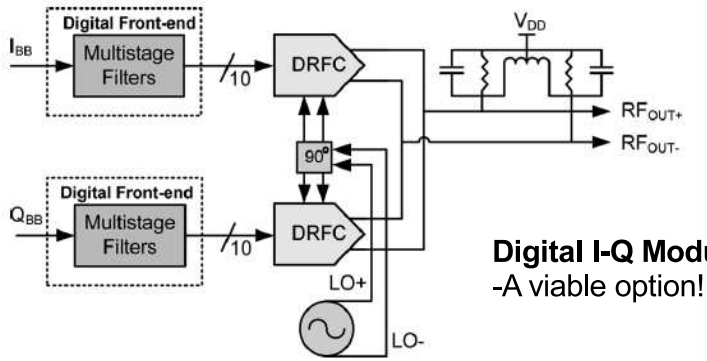
Polar (Kahn) TX
-Extended BW
-Phase resolution
-Path mismatch



Outphasing (Chirex) TX
-Phase resolution
-Output Combiner



BP-DSM TX
-OSR Limitation
-High-Q Filter needed



Digital I-Q Modulator
-A viable option!

Proposed Architecture

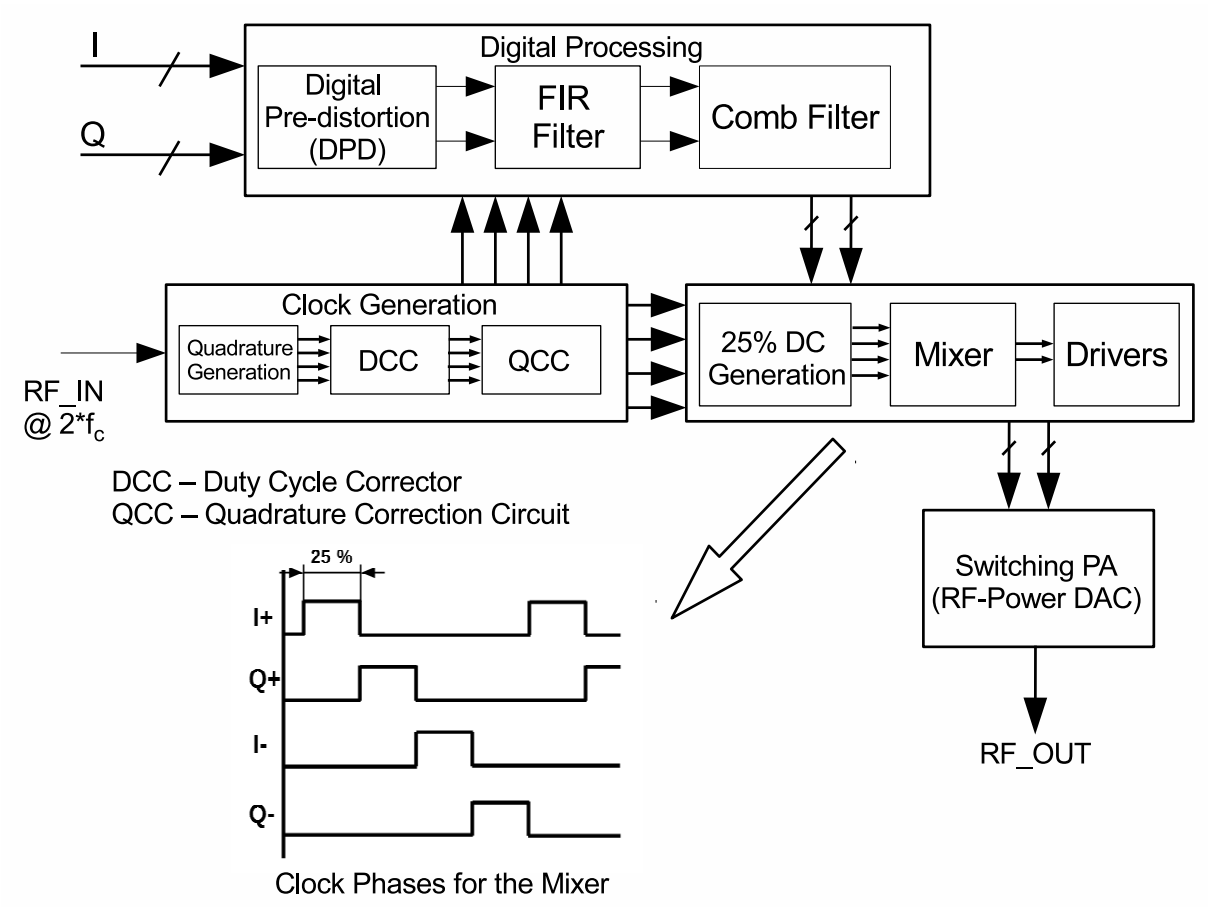


Figure : Detailed system diagram of the proposed transmitter

- Digital inputs – I and Q data streams (9-bits wide each)
- RF Input – Continuous wave signal at $2 \times f_c$.
- Clock generation block – generates differential rail-to-rail quadrature clock phases.
- Digital processing block – DPD, 2 levels of filtering.
- Digital mixing
- Tunable RF Power DAC as the output stage.

Proposed Digital Filtering

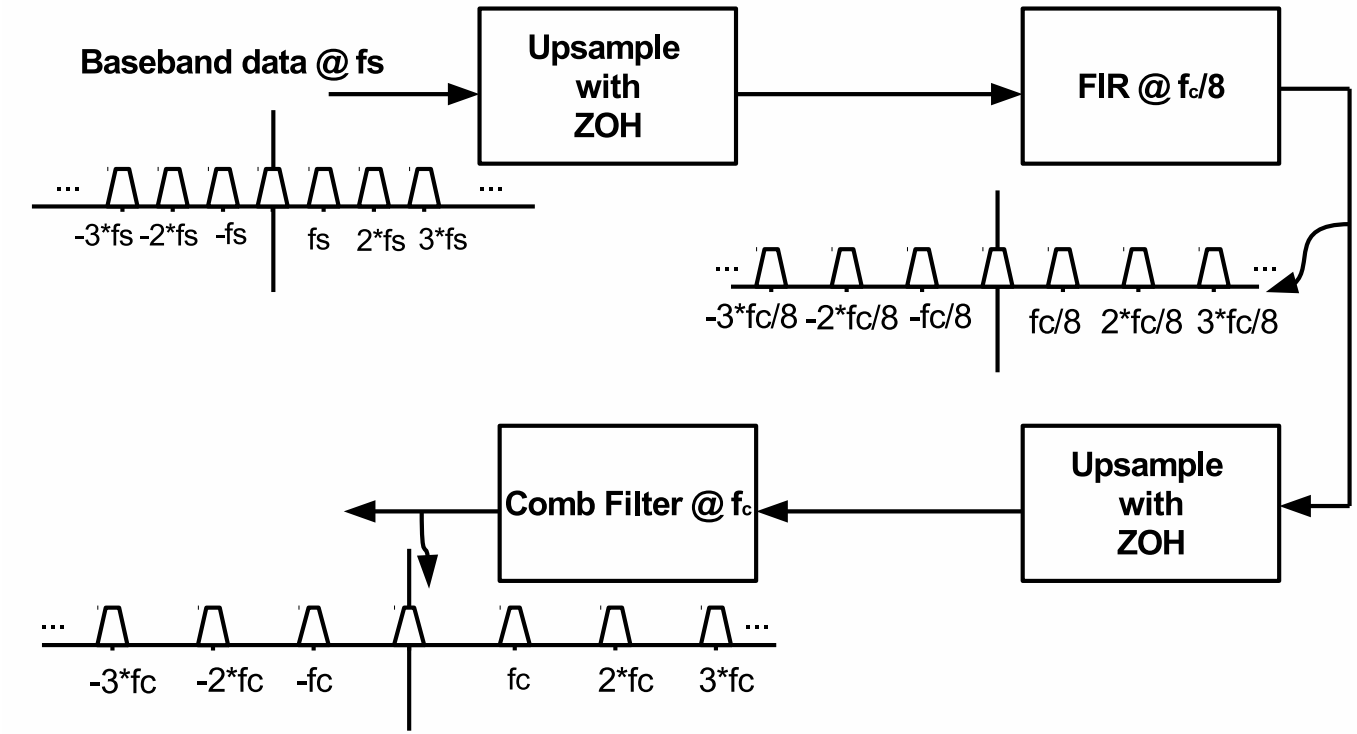


Figure : Digital processing of the input signal for spur suppression

- 2 stages of up-sampling with filtering

Measured Result – Transmitting a 16 QAM Signal

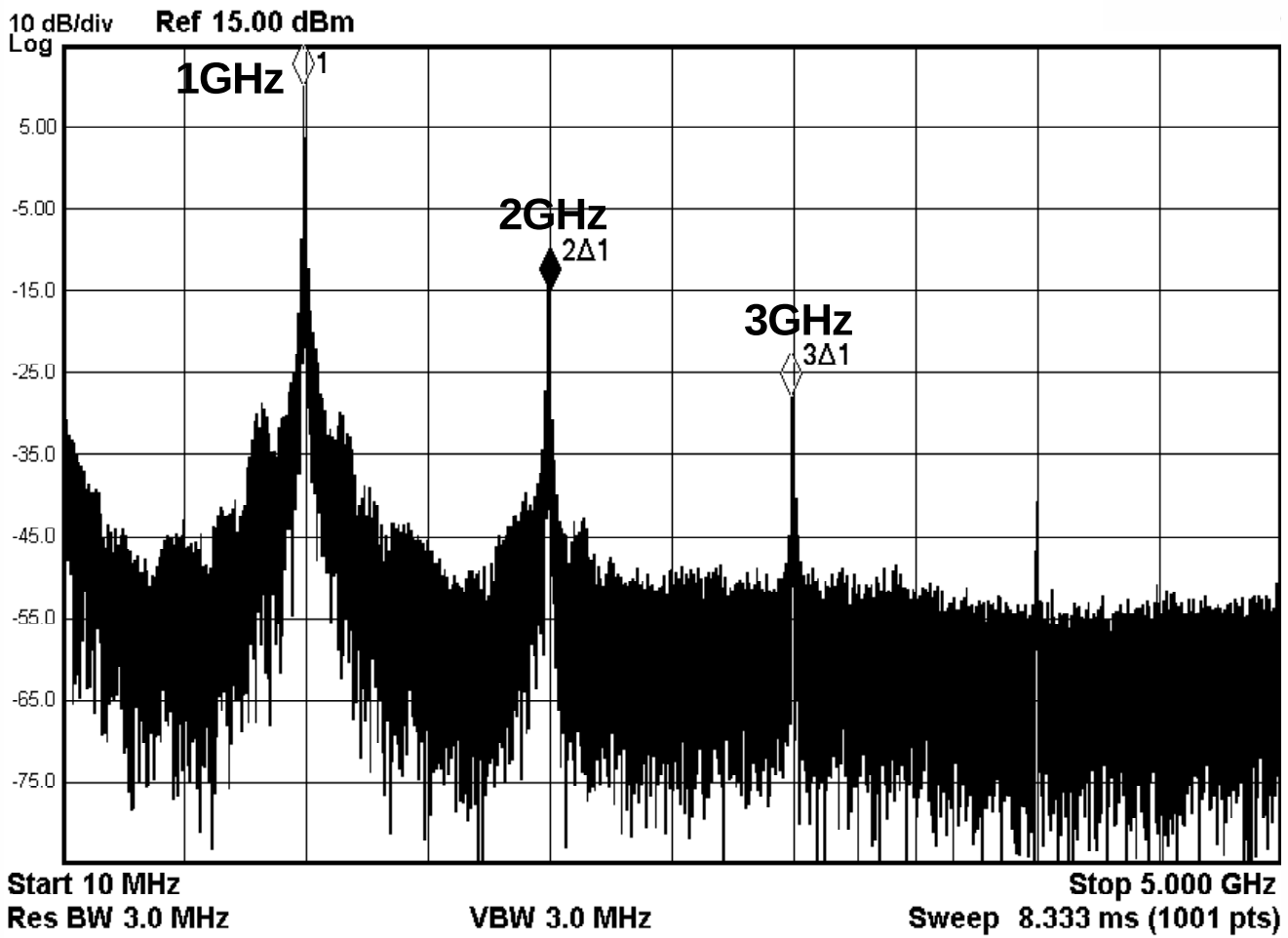


Figure : Wideband spectrum while transmitting at 1 GHz. The spurs exist only at the harmonics of 1 GHz. The other spurs are cleaned up by the digital processing block.

Clock Generation

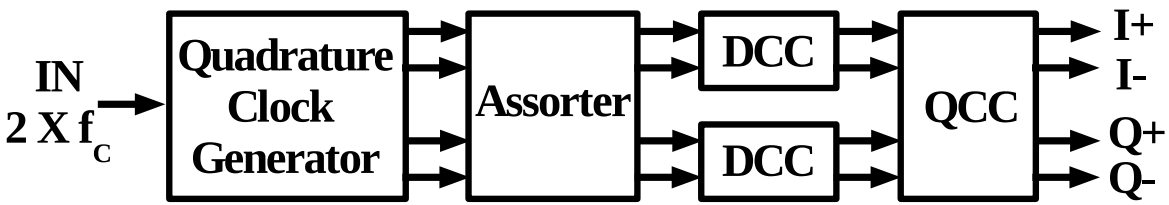


Figure : Quadrature clock generation and correction scheme. DCC: Duty Cycle Corrector. QCC: Quadrature Correction Circuit

- The input CW signal at $2 \times f_c$ is converted to differential rail-to-rail quadrature signals.
- Duty cycle and quadrature impairments arise due to mismatches and PVT variations – need real-time correction
- Assorter to identify the I phase, Q phase and their complements.
- 2 DCC circuits correct the I and Q phases to have 50% duty cycle.
- QCC corrects the quadrature error.
- DCC and QCC need to function across the entire frequency range – require wide frequency range DCC and QCC circuits.

Duty Cycle Correction

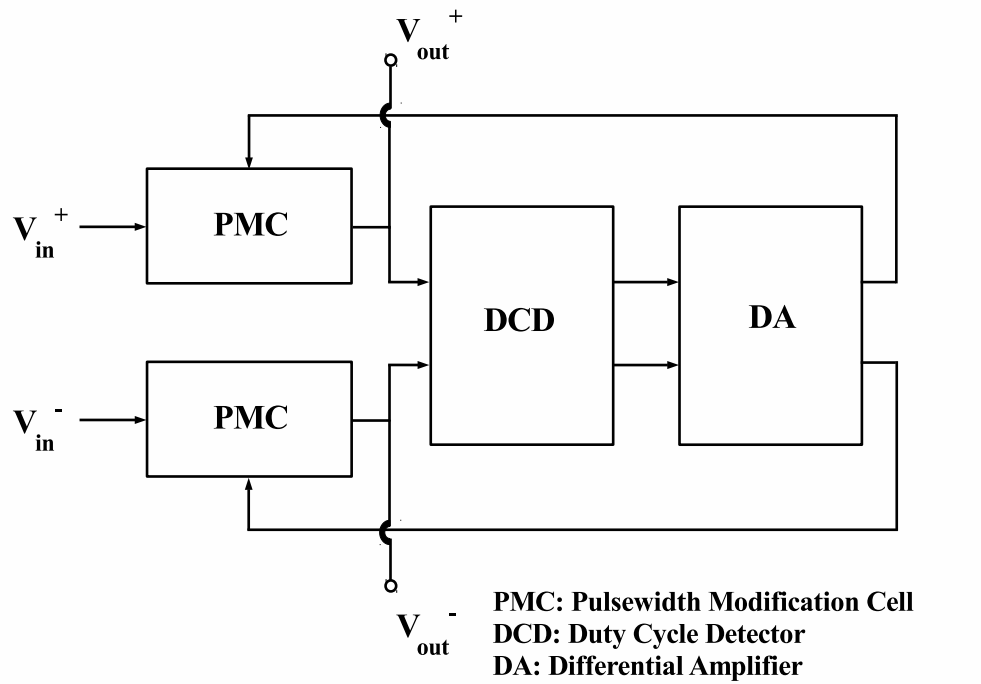


Figure : Architecture of the Duty Cycle Corrector

- Analog negative feedback loop to correct duty cycle errrors.
- Duty cycle detector (DCD) – operates on differential clock phases – DC average.
- Pulsewidth Modification Cell (PMC) – changes the duty cycle according to the control voltage.
- Differential Amplifier – for gain and biasing the control voltage.

"A 0.13.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 5, pp. 1975-1983, May 2016.

Quadrature Correction Circuit

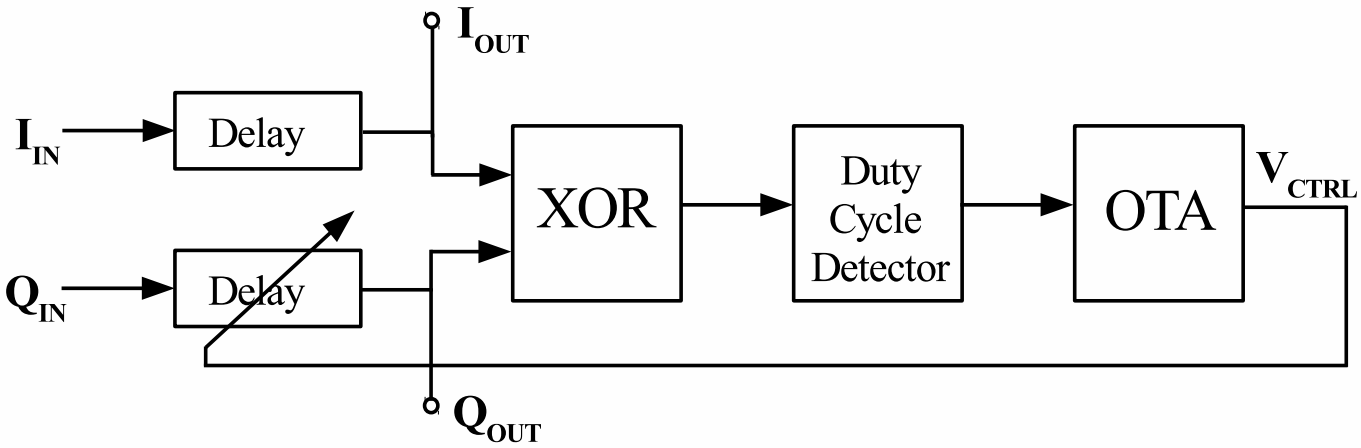


Figure : Architecture of the quadrature correction loop.

- Fixed delay in the I path and a variable delay in the Q path.
- Quadrature error converted to duty cycle error using an XOR.
- Perfect quadrature implies 50% duty cycle at the XOR output
- Analog negative feedback loop which adjusts the delay on the Q path to optimize for 50% duty cycle at the output of the XOR.

"A 0.1 to 2 GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 3, pp. 1044-1053, March 2017.

Digital Mixing

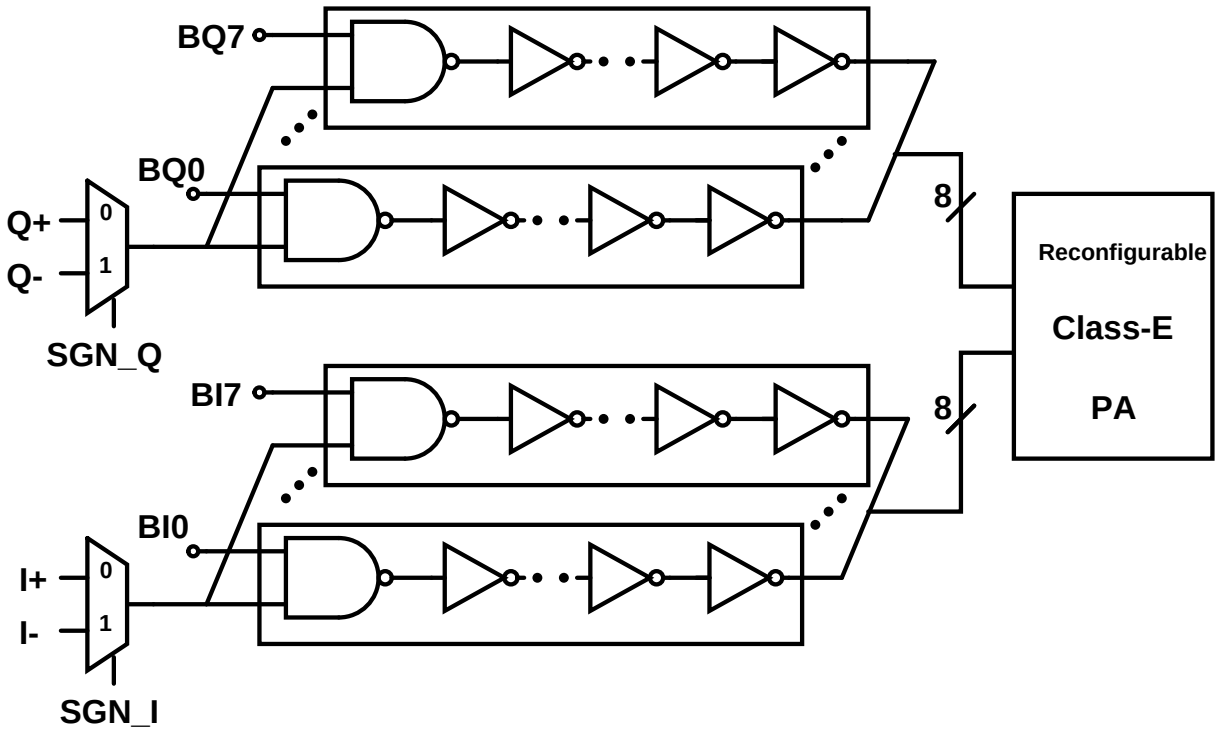
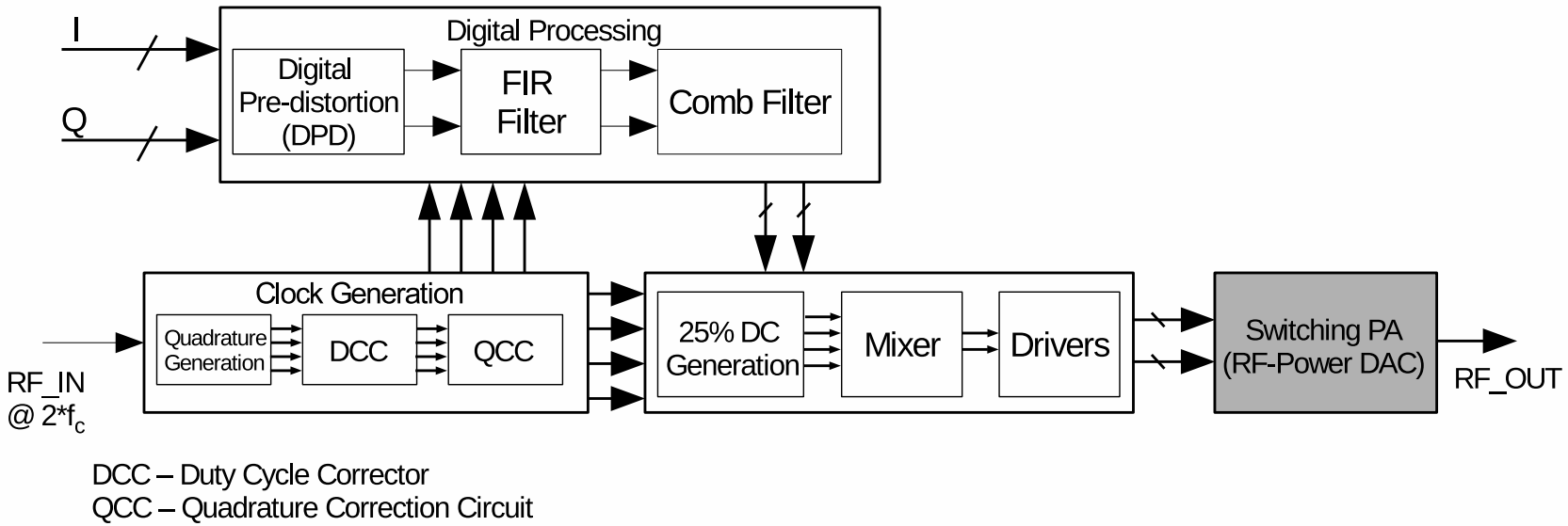


Figure : Schematic of the mixer and drivers

- Mixing using NAND gates.
- 25% duty-cycle clocks used to obtain effective 50% ON/OFF time at the PA.
- Complementary phase selected for negative data values.

Reconfigurable Class-E Power Amplifier Design

"A 0.75 2.5 GHz All-Digital RF Transmitter with a Tunable Integrated Class-E Power Amplifier for SDR/CR" *Immanuel Raja, Gaurab Banerjee*. (Manuscript under preparation.)



Traditional Class-E Implementation

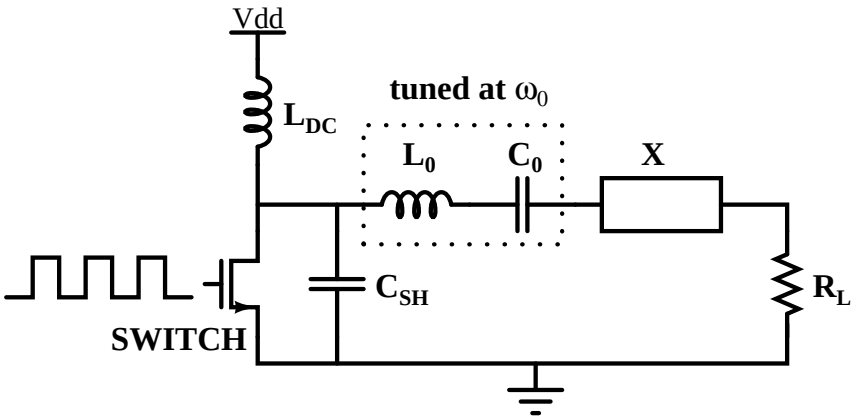


Figure : Traditional Class-E power amplifier schematic.

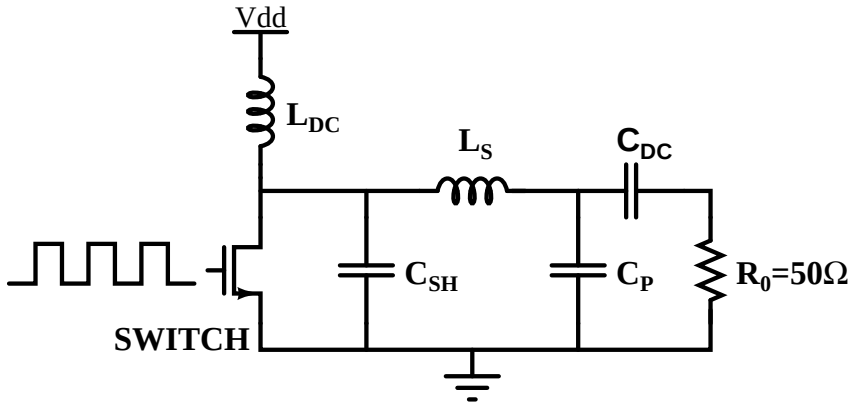


Figure : Implementation of a Class-E power amplifier showing the impedance transformation network.

$$Z_L = \frac{R_0}{1+(\omega R_0 C_P)^2} + j\left(\omega L_S - \frac{\omega R_0^2 C_P}{1+(\omega R_0 C_P)^2}\right)$$

$$\begin{aligned} R_L &= 0.5768\frac{V_{DD}^2}{P_{OUT}} \\ C_{SH} &= 0.1836\frac{1}{\omega R_L} \\ X &= 1.152 R_L \end{aligned}$$

The component values are calculated as follows:

$$\begin{aligned} C_P &= \frac{1}{\omega R_0}\sqrt{\frac{R_0}{R_L}-1} \\ L_S &= \frac{1}{\omega}\left(X + \frac{\omega R_0^2 C_P}{1+(\omega R_0 C_P)^2}\right) \end{aligned}$$

Component Values for a Traditional Class-E PA

$P_{OUT} = 18$ dBm $R_L = 18\Omega$ $V_{DD} = 1.5$ V

Frequency	C_P	L_S	C_{SH}
750 MHz	5.08 pF	10.25 nH	1.89 pF
800 MHz	4.76 pF	9.6 nH	1.77 pF
1 GHz	3.8 pF	7.68 nH	1.42 pF
1.5 GHz	2.54 pF	5.12 nH	947 fF
2 GHz	1.9 pF	3.84 nH	710 fF
2.5 GHz	1.52 pF	3.07 nH	568 fF

- L_S varies from 3nH to 10.25nH which is impossible to synthesize on-chip.
- Using a varactor tuned secondary to change the effective inductance of the primary in a transformer – very less inductance range.
- Need to design Class-E PAs with a fixed L_S over a wide frequency range.

Parameterized Class-E Equations

$$
\begin{aligned}
K_L &= \frac{\omega L_{DC}}{R_L} \\
K_C &= \omega C_{SH} R_L \\
K_P &= \frac{P_{OUT} R_L}{V_{DD}^2} \\
K_X &= \frac{X}{R_L}
\end{aligned}
$$

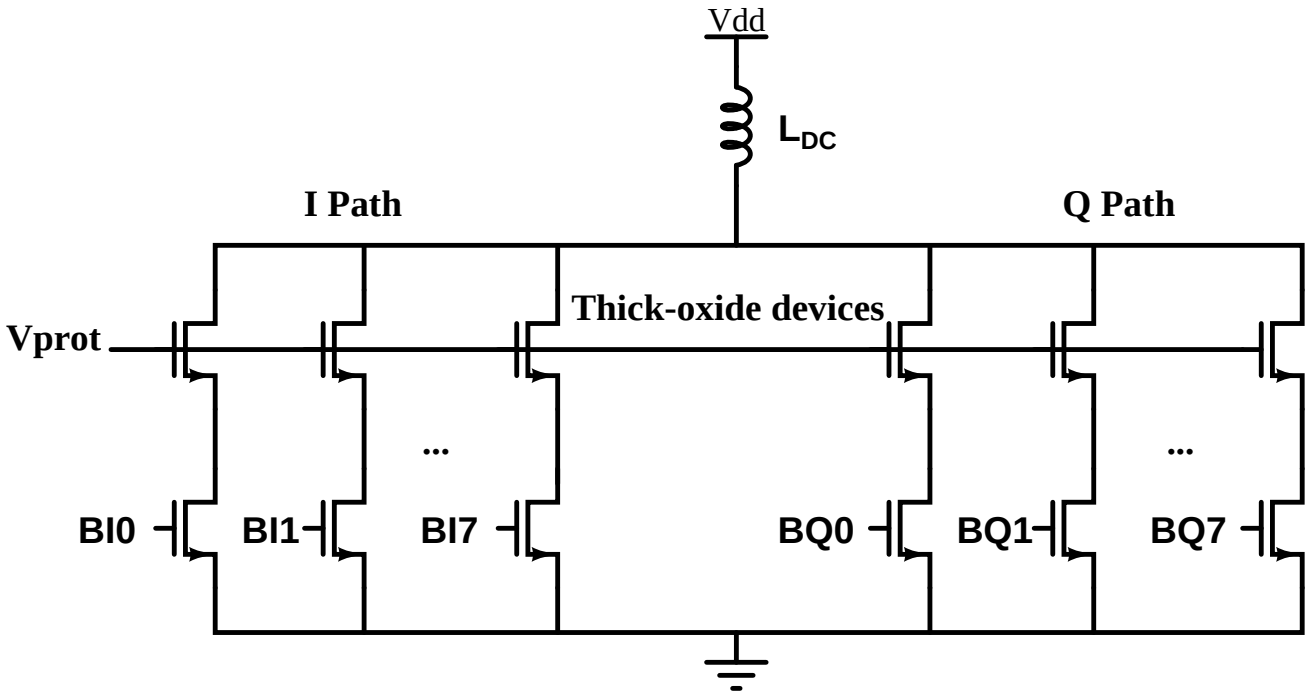
Table : Design set for $(1 < q < 1.65)$

$$
\begin{aligned}
K_L(q) &= 8.085q^2 - 24.53q + 19.23 \\
K_C(q) &= -6.97q^3 + 25.93q^2 - 31.071q + 12.48 \\
K_P(q) &= -11.90q^3 + 42.753q^2 - 49.63q + 19.70 \\
K_X(q) &= -2.9q^3 + 8.8q^2 - 10.2q + 5.02
\end{aligned}
$$

M. Acar, A. J. Annema, and B. Nauta, "Analytical design equations for class-E power amplifiers," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 54, no. 12, pp. 27062717, 2007.

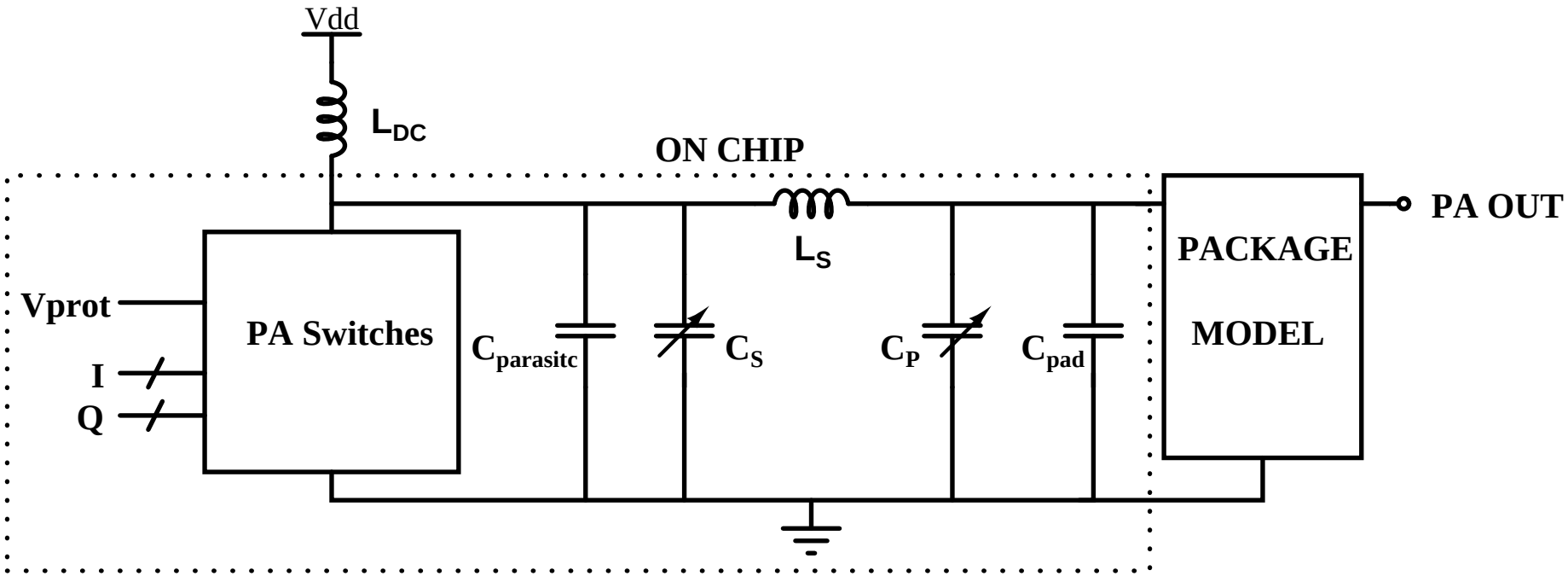
- Class-E PA variable set: $\{P_{OUT}, V_{DD}, L_{DC}, R_L, X, C_{SH}\}$.
- Variable set for the current implementation: $\{P_{OUT}, V_{DD}, L_{DC}, C_P, L_S, C_{SH}\}$.
- For a wideband reconfigurable PA, L_S, L_{DC} and V_{DD} are constant across the frequency range.
- P_{OUT} is expected to be constant across the frequency range with some tolerance.
- Variables are: $\{C_P, C_{SH}\}$

Digital-to-RF Conversion – RF-DAC



- Binary-weighted switches form the switch of the PA.
- 25% duty cycle for I and Q paths such that the maximum ON period of the total switch is 50%.
- Binary-weighted thick oxide devices for protecting the switching transistors.
- V_{prot} chosen such that resistance of the thick oxide transistor is minimized and bottom device is protected at the same time.

PA Implementation



$V_{DD} = 1.5V$, $L_S = 3.5nH$, $L_{DC} = 5nH$

Frequency	C_P	C_{SH}	Impedance
750 MHz	5.5 pF	3.5 pF	$22.83 - j9.56$
1 GHz	5 pF	3 pF	$17.6 - j2.83$
1.5 GHz	3.5 pF	1.5 pF	$16.43 + j6.5$
2 GHz	2 pF	0.5 pF	$18.56 + j19.96$
2.5 GHz	1 pF	0 pF	$19.3 + j20.33$

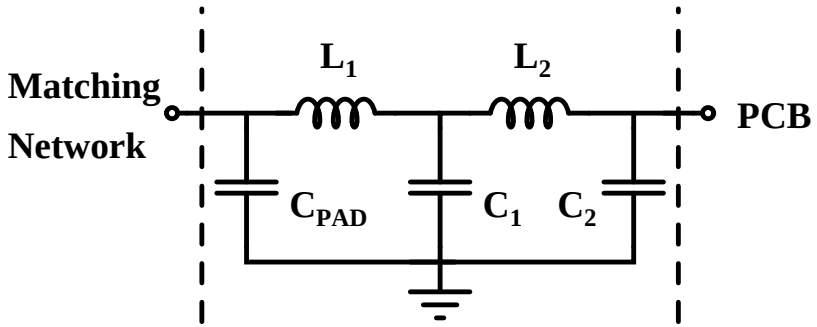
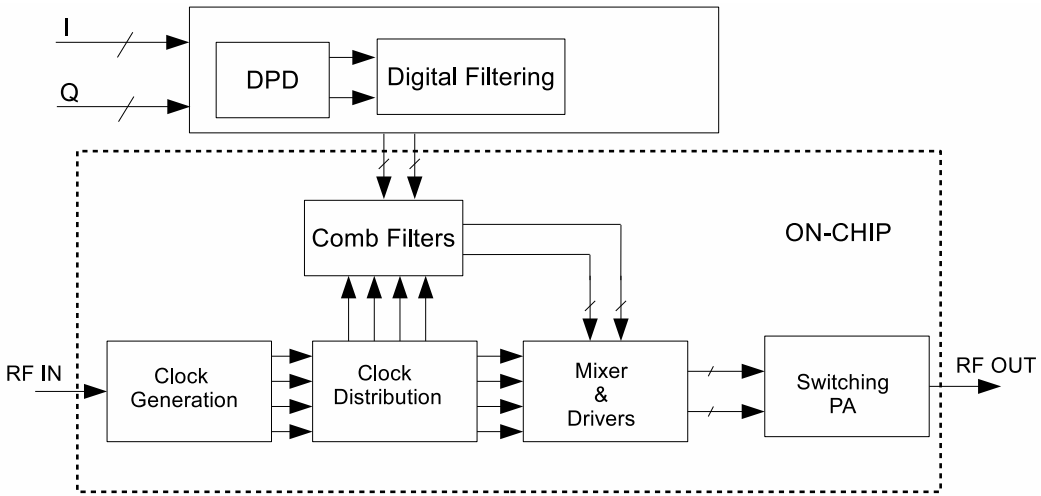


Figure : A typical packaging model.

Chip Details



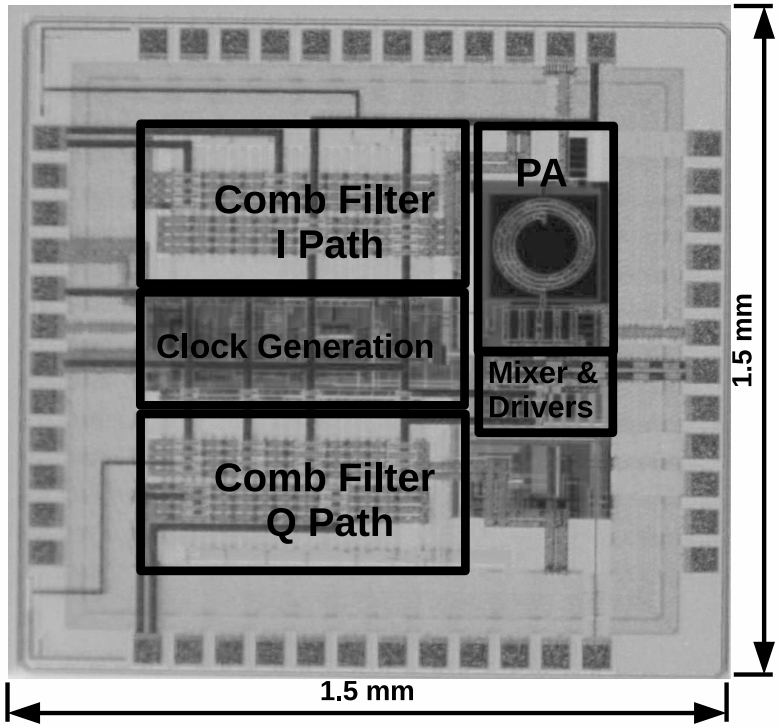
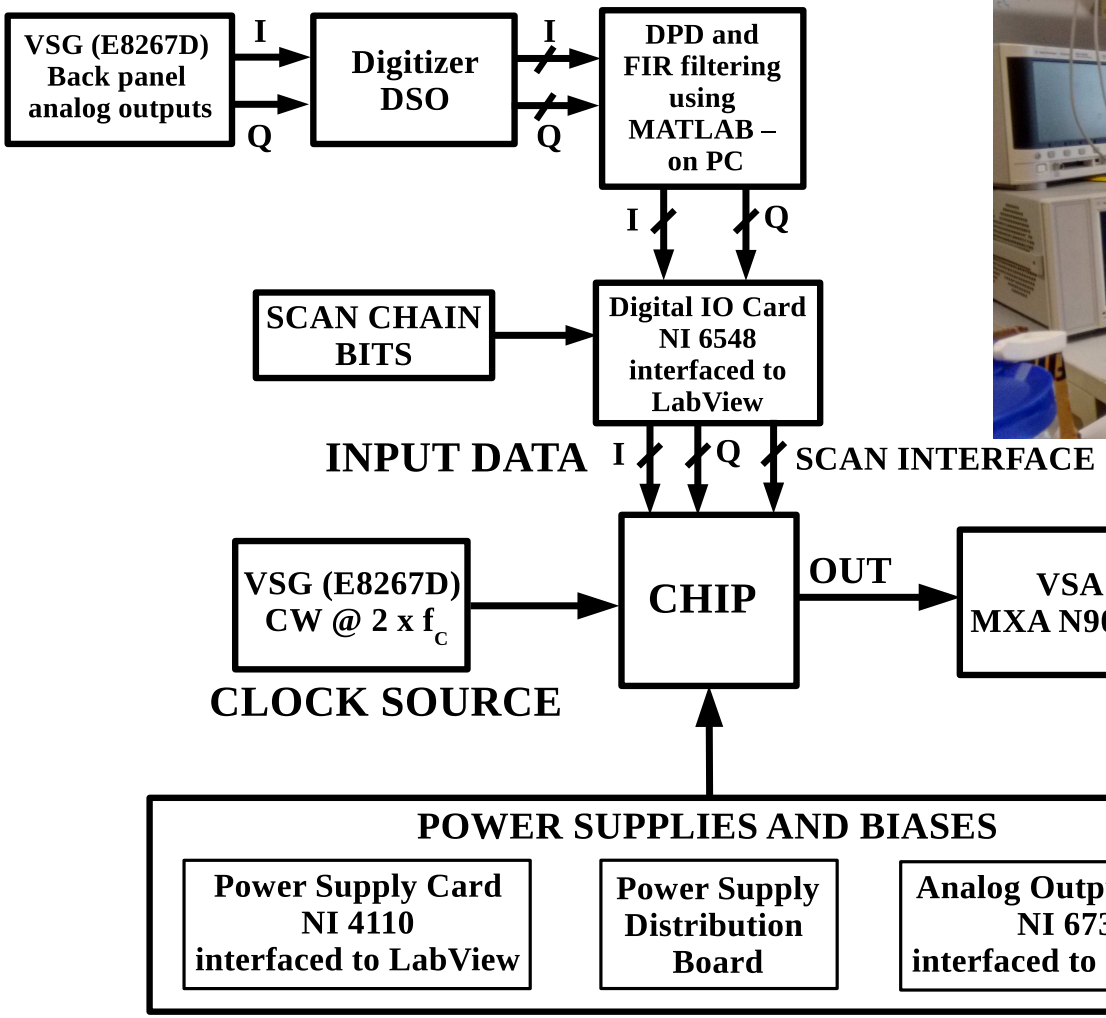
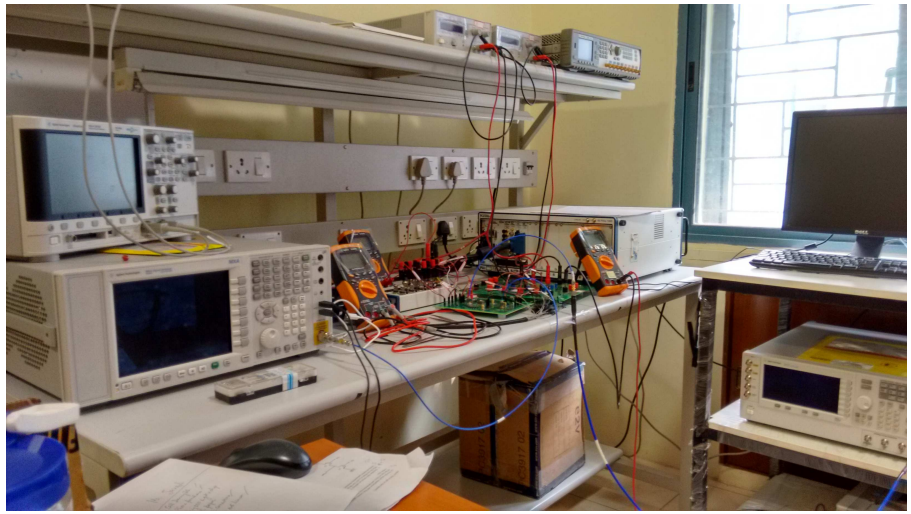


Figure : Chip micrograph.

- Fabricated in UMC 130nm RFCMOS process (8 metal layers).
- Active area: $1mm \times 1mm$.
- Packaged in a QFN48 .
- Digital Pre-distortion (DPD), FIR filtering, DC feed inductor implemented off-chip.

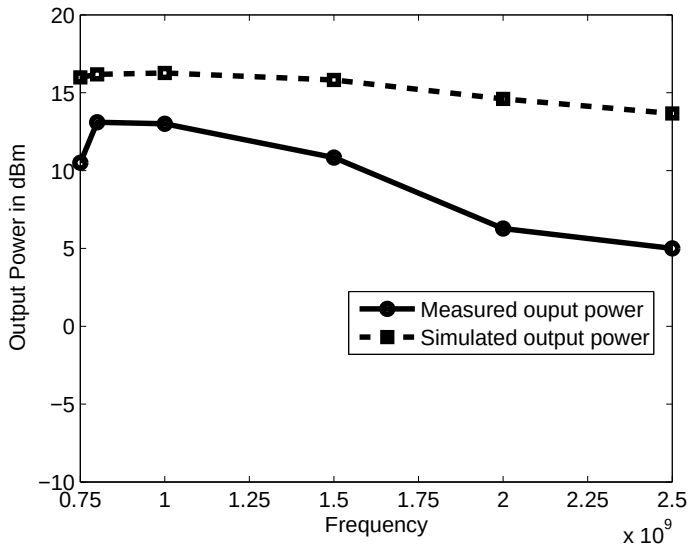
Experimental Setup for Test and Measurement



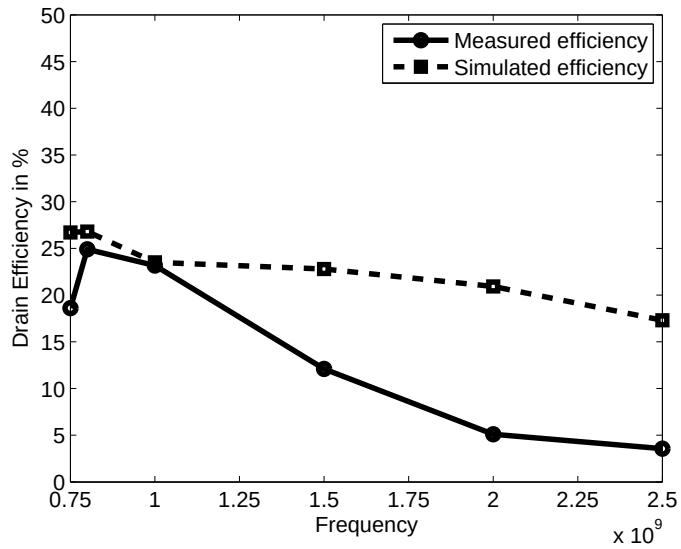


Measured Results

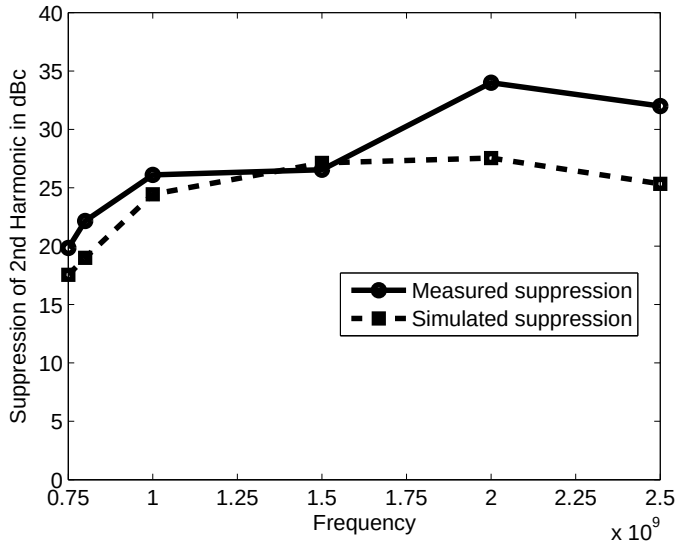
Output Power



Efficiency



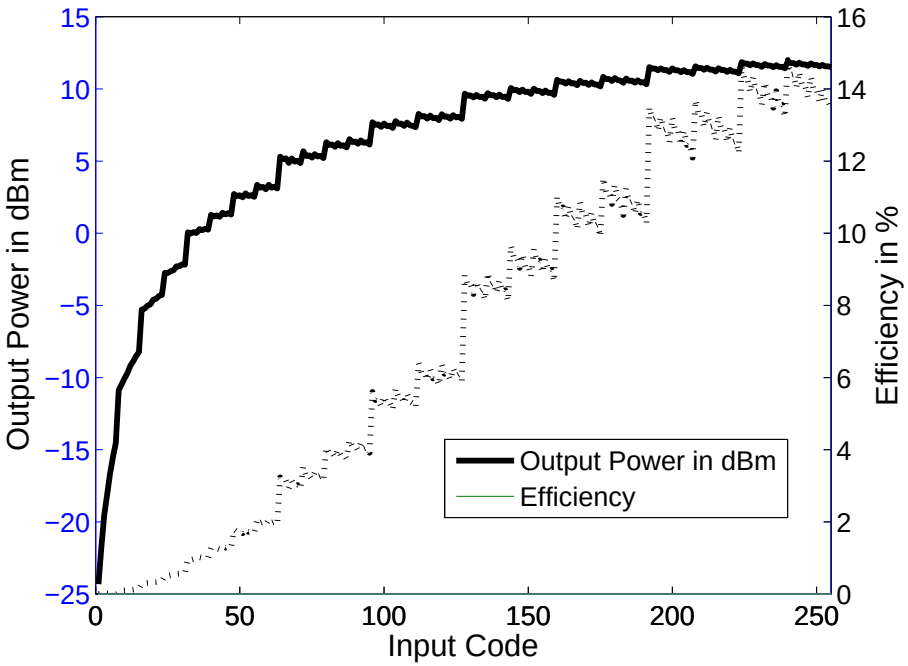
2^{nd} harmonic suppression

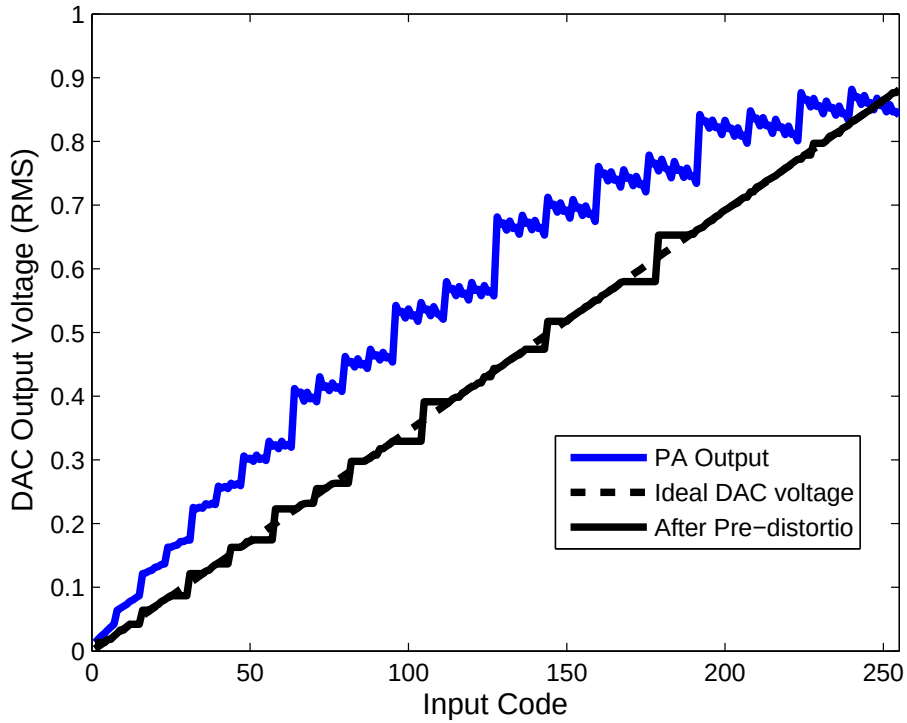


Reasons for discrepancies between simulated and measured performance:

- Inductor performance.
- Off-chip placement of the DC Feed inductor.
- High frequency slew degradation at possibly slow corner, high temperature operation.

Measured Results – DAC Performance and Digital Pre-distortion (DPD)





- End-fit linearization for the DAC.
- Mapping the equivalent voltage characteristics to a straight line.
- Jumps at MSB transitions can be avoided by using thermometer encoding.

Measured Results – Transmitting a 16 QAM Signal

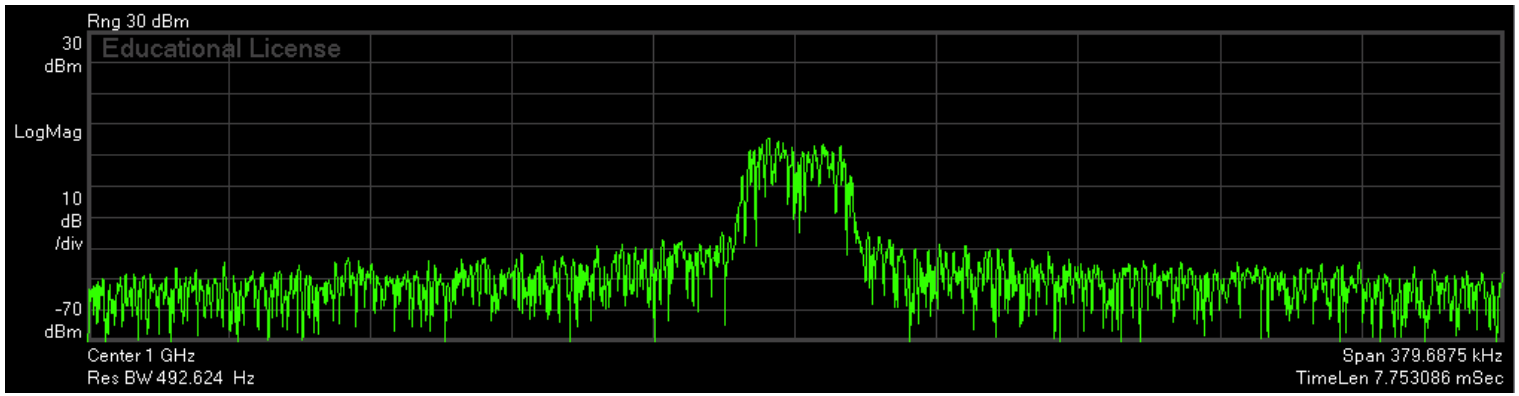
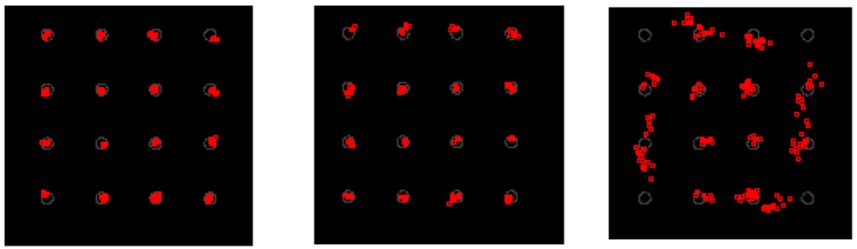


Figure : Close-up spectrum while transmitting a 16-QAM signal at 1 GHz.



800 MHz 1 GHz 2 GHz

Frequency	800 MHz	1 GHz	2 GHz
EVM (RMS)	3.1%	4%	13.4%
Magnitude Error	1.6%	1.9%	8.3%
Phase Error	2.15 deg	3.5 deg	10.4 deg
Quadrature Error	0.7 deg	1.1 deg	3.6 deg
Gain Imbalance	0.3 dB	0.3 dB	0.14 dB

Comparison with the State-of-the-Art

Reference	Yin2015	Ingels2010	**This work**
PA Class	Class-AB Buffer	Common Source Pre-power amplifier	Class E
Frequency Range	4-band solution between 0.1 to 6 GHz (0.1-0.7, 0.7-1.4, 1.2-3.2, 3-6) GHz	0.75 - 2.5 GHz	0.75 - 2.5 GHz
Output Power	2dBm	0-4 dBm	5-13 dBm
Efficiency	–	–	8-14%
EVM	2.3% @ 1.7dBm, LTE20 QPSK	3.2% @ 0dBm	4% for 16-QAM at 1 GHz without backoff
Technology	65nm CMOS	40nm CMOS	130nm CMOS
V_{DD}	2.5V	2.5V	1.5V
Area	$2.2 \times 0.95mm^2$	$1.3mm^2$	$1mm^2$

Conclusion

Key Contributions

A fully integrated CMOS transmitter and power amplifier for SDR has been designed and developed.

The main contributions to the field as presented in this thesis are as follows:

- Differential quadrature clock generation across a wide frequency range from a single-ended CW input at twice the carrier frequency.
- Architectural solutions for suppression of spurious components arising due of sampling of digital signals.
- Duty cycle correction (DCC) circuit working across the entire frequency range.
- An alternate duty cycle measurement algorithm. Using frequency domain information of the signal up to the third harmonic, time domain information like duty cycle, rise and fall times can be calculated.

Key Contributions (Contd.)

- Quadrature correction circuit functional across the entire frequency range.
- Development of theory and design methodology for a reconfigurable Class-E PA, with a single fixed series inductor. The PA is reconfigured through capacitor banks.
- Design of CMOS power amplifier that can span this wide frequency range with sufficient output power and efficiency, uniformly across the frequency range, supporting varying envelope complex modulation signals, with good linearity across the frequency range.
- Digital power control over the frequency range of interest.
- Digital pre-distortion scheme for the designed PA.

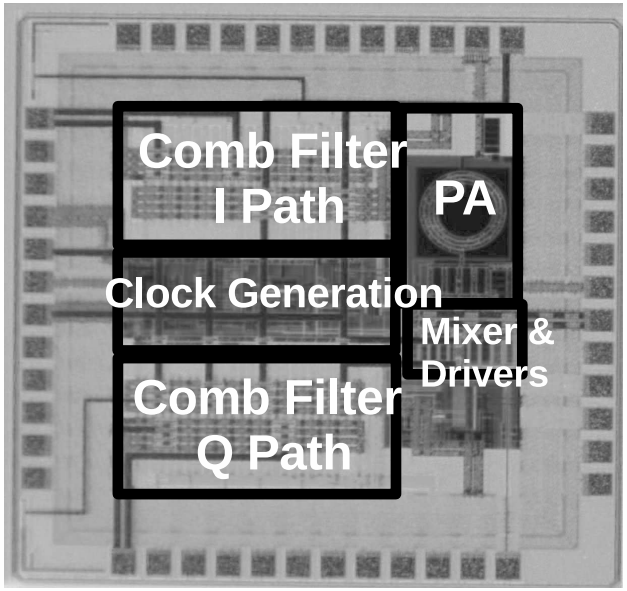
The proposed transmitter is the first reported wide-range all digital RF transmitter with an integrated tunable Class-E PA which can support non-constant envelope complex modulation.

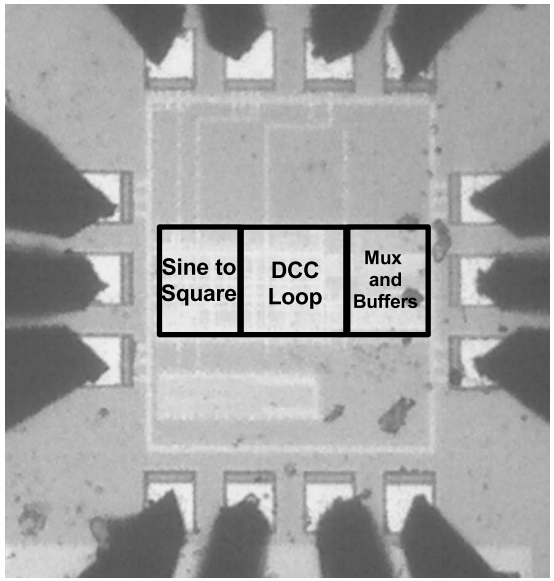
Publications

- I. Raja; G. Banerjee; M. A. Zeidan; J. A. Abraham, "A 0.1-3.5-GHz Duty-Cycle Measurement and Correction Technique in 130-nm CMOS," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , (Accepted/In press - Oct 8 2015 – Early Access)
- I. Raja, V. Khatri, Z.Zaira, G. Banerjee, "A 0.1 to 2 GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS" *Submitted to IEEE Transactions on Very Large Scale Integration (VLSI) Systems*
- I. Raja, G. Banerjee, "A 0.75 2.5 GHz All-Digital RF Transmitter with a Tunable Integrated Class-E Power Amplifier for SDR/CR" (Manuscript under preparation.)

Fabricated Chips

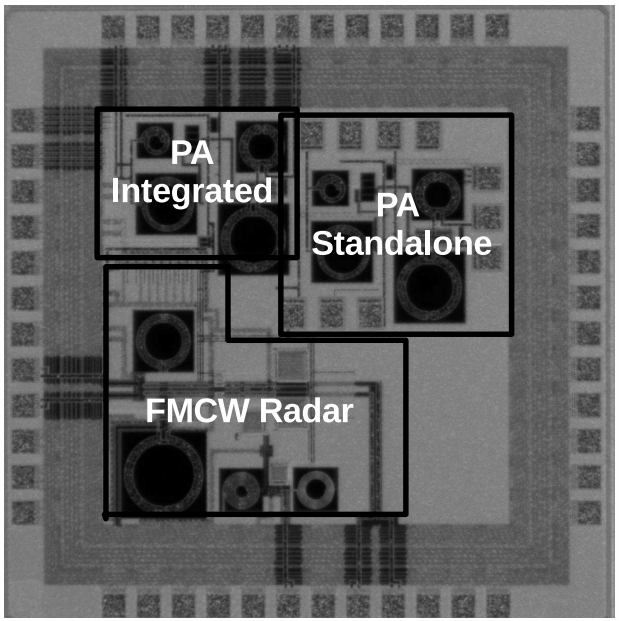
Transmitter with PA for SDR

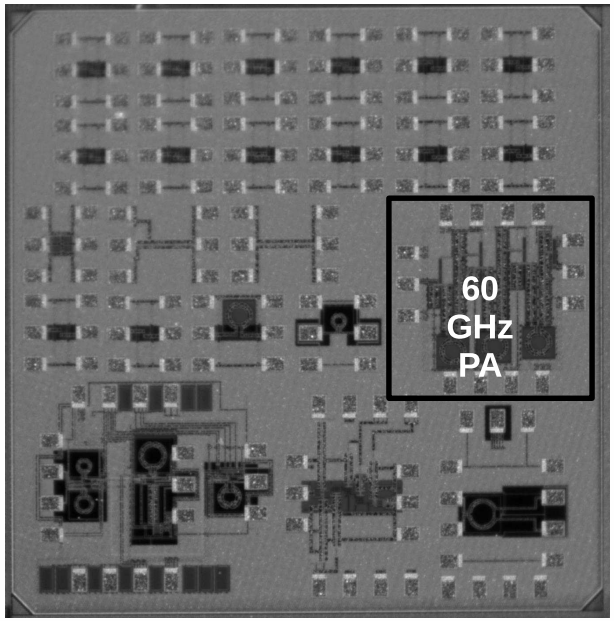




DCC Test Circuit

10 GHz RADAR Chip with an integrated PA and a standalone 10 GHz PA





60 GHz PA

Future Directions

- Thermometer implementation of the DAC – to improve linearity and monotonicity.
- Better modelling of passives and interconnects.
- Use of differential architecture to suppress the 2^{nd} harmonic content.
- Implementation in advanced technology nodes – lesser power consumption by digital blocks, clock and driver circuitry.
- Implementation in advanced technology nodes – more stacking of the PA transistors – higher supply voltages – higher output power.

Thank You